DSP56305

Advance Information

SINGLE CHIP CHANNEL CODEC DIGITAL SIGNAL PROCESSOR

Motorola designed the DSP56305 to deliver the high performance required to support Global System for Mobile (GSM) communications applications that use digital signal processing to perform channel equalization, channel coding, and speech coding. By combining three dedicated on-chip hardware co-processors (filter, Viterbi, and cyclic code) with a DSP56300 core, the DSP56305 performs all the complex signal processing required by a single Radio Frequency (RF) carrier in one chip, satisfying the demand for high integration at a low cost. The DSP56300 core includes an on-chip PLL, a Data ALU, an instruction cache, on-chip debugging modules, on-chip program and data memory, six DMA channels, and an external memory expansion port. In addition to the co-processors, the DSP56305 provides two types of serial ports, a PCI/Universal bus 32-bit Host Interface, and timers (see **Figure 1**). The DSP56305 provides an industry-leading performance rate of 80 MIPS at 3.3 V.

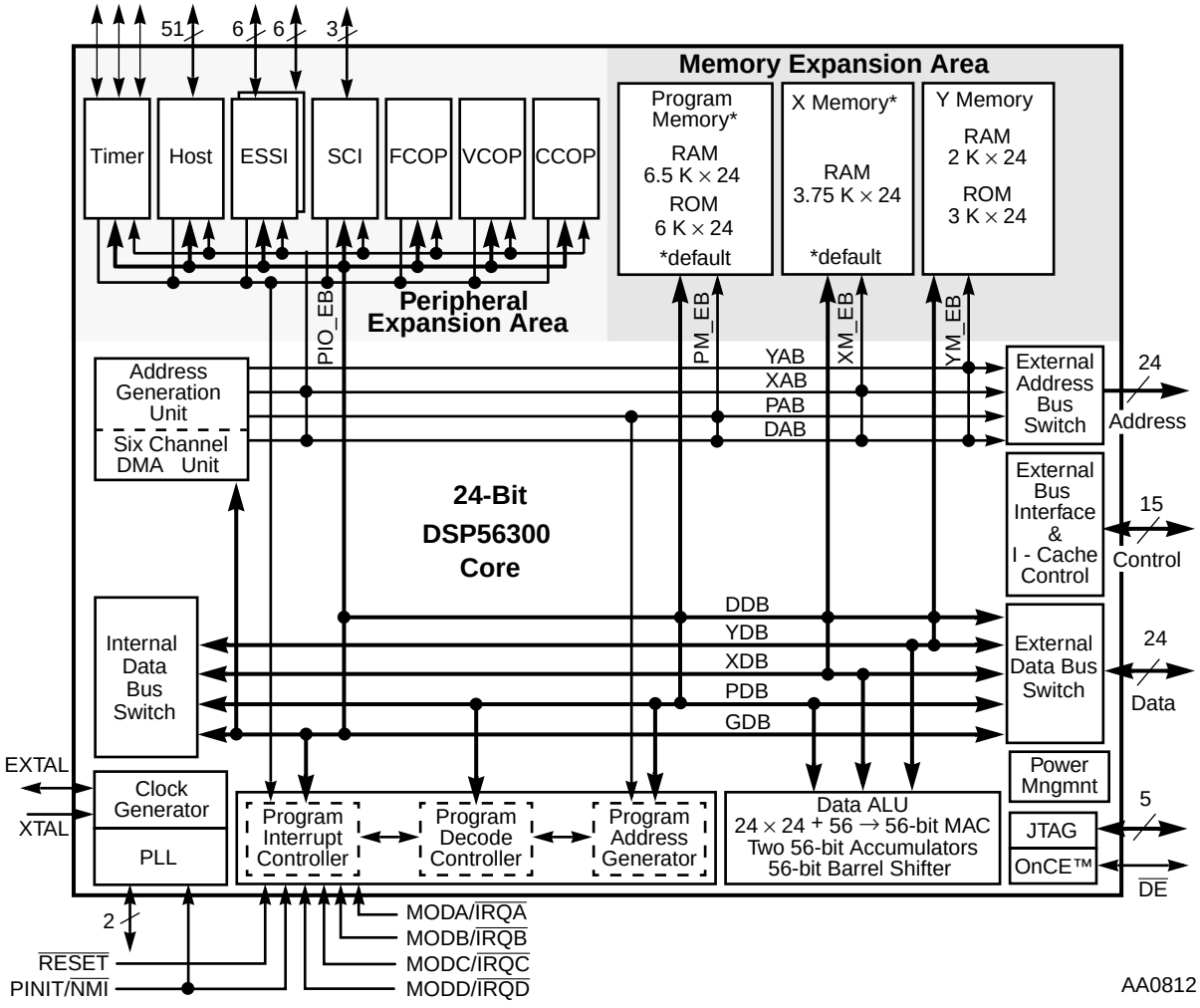

Figure 1 DSP56305 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56305 FEATURES

- High performance DSP56300 core
  - 80 Million Instructions Per Second (MIPS) with an 80 MHz clock at 3.3 V
  - Object code compatible with the DSP56000 core
  - Highly parallel instruction set
  - Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
  - 56-bit parallel barrel shifter
  - 24-bit or 16-bit arithmetic support under software control
  - Position independent code support
  - Addressing modes optimized for DSP applications
  - On-chip instruction cache controller
  - On-chip memory-expandable hardware stack
  - Nested hardware DO loops
  - Fast auto-return interrupts
  - On-chip concurrent six-channel Direct Memory Access (DMA) controller
  - On-chip Phase Lock Loop (PLL) and clock generator
  - On-Chip Emulation (OnCE™) module
  - JTAG Test Access Port (TAP)
  - Address Tracing mode reflects internal accesses at the external port
  - 21 mm × 21 mm, 252-pin PBGA package
  - Pin-compatible in 252-pin PBGA package with the DSP56301
- On-chip memories
  - Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data Ram Size
disabled	disabled	6656 × 24-bit	0	3840 × 24-bit	2048 × 24-bit
enabled	disabled	5632 × 24-bit	1024 × 24-bit	3840 × 24-bit	2048 × 24-bit
disabled	enabled	7680 × 24-bit	0	2816 × 24-bit	2048 × 24-bit
enabled	enabled	6656 × 24-bit	1024 × 24-bit	2816 × 24-bit	2048 × 24-bit

  - 6144 × 24-bit Program ROM
  - 3072 × 24-bit Y data ROM
  - 192 × 24-bit bootstrap ROM

- Off-chip memory expansion
  - Data memory expansion to two 16 M x 24-bit word memory spaces
  - Program memory expansion to one 16 M x 24-bit word memory space
  - External memory expansion port
  - Chip select logic provides glueless interface to SRAMs and SSRAMs
  - On-chip DRAM controller provides glueless interface to DRAMs
- On-chip peripherals
  - PCI Rev. 2.1-compliant 32-bit parallel PCI/Universal Host Interface (HI32) with glueless interface to other DSP563xx buses
  - ISA interface requires only 74LS45-style buffer
  - Two Enhanced Synchronous Serial Interfaces (ESSI)
  - Serial Communications Interface (SCI) with baud rate generator
  - Triple timer module
  - Up to forty-two programmable General Purpose Input/Output pins (GPIO), depending on which peripherals are enabled
- On-chip co-processors
  - Filter Co-Processor (FCOP) implements a wide variety of convolution and correlation filtering algorithms. In GSM applications, the FCOP cross-correlates between the received training sequence and a known midamble sequence to estimate the channel impulse response, and then performs match filtering of received data symbols using coefficients derived from that estimated channel.
  - Viterbi Co-Processor (VCOP) implements Maximum Likelihood Sequential Estimation (MLSE) algorithm for channel decoding and equalization (uplink) and channel convolution coding (downlink). The VCOP supports constraint lengths (k) of 4, 5, 6, or 7 with number of states 8, 16, 32, or 64, respectively; code rates of 1/2, 1/3, 1/4, or 1/6; and trace-back Trellis depth of 36.
  - Cyclic-code Co-Processor (CCOP) executes cyclic code calculations for data ciphering and deciphering, as well as parity code generation and check. The CCOP is fully programmable and not dedicated to a specific algorithm, but it is well suited for GSM A5.1 and A5.2 data ciphering algorithms. The CCOP can generate mask sequences for data ciphering, and supports Fire encode and decode for burst error correction, as well as generation of Cyclic Redundancy Code (CRC) syndrome for any polynomial of any degree up to 48.
- Reduced power dissipation
  - Very low power CMOS design
  - Wait and Stop low power standby modes
  - Fully-static logic, operation frequency down to DC
  - Optimized power management circuitry

PRODUCT DOCUMENTATION

The three documents listed in **Table 1** are required for a complete description of the DSP56305 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the Motorola DSP home page on the Internet, which will have the latest information (see its address below).

Table 1 DSP56301 Documentation

Topic	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family architecture, 24-bit core, and instruction set	DSP56300FM/AD
DSP56305 User's Manual	Detailed description of DSP56305 memory, peripherals, and interfaces	DSP56305UM/AD
DSP56305 Technical Data	DSP56305 pin and package descriptions, and electrical and timing specifications	DSP56305/D

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