DSP56304

Advance Information
24-BIT DIGITAL SIGNAL PROCESSOR

Motorola designed the ROM-based DSP56304 to support multifunction wireless and embedded DSP applications. In addition to the large on-chip ROM spaces, the DSP56304 also has a ROM patch feature that facilitates updates to the mask-program ROM-based on-chip software. The DSP56304 includes a triple timer module, Host Interface (HI08), an Enhanced Synchronous Serial Interface (ESSI), and a Serial Communications Interface (SCI). The DSP56300 core family includes a Phase Lock Loop (PLL), External Memory Interface (EMI), Data Arithmetic Logic Unit (Data ALU), 24-bit addressing, instruction cache, and DMA. The DSP56304 offers 66/80 MIPS using an internal 66/80 MHz clock at 3.0–3.6 volts.

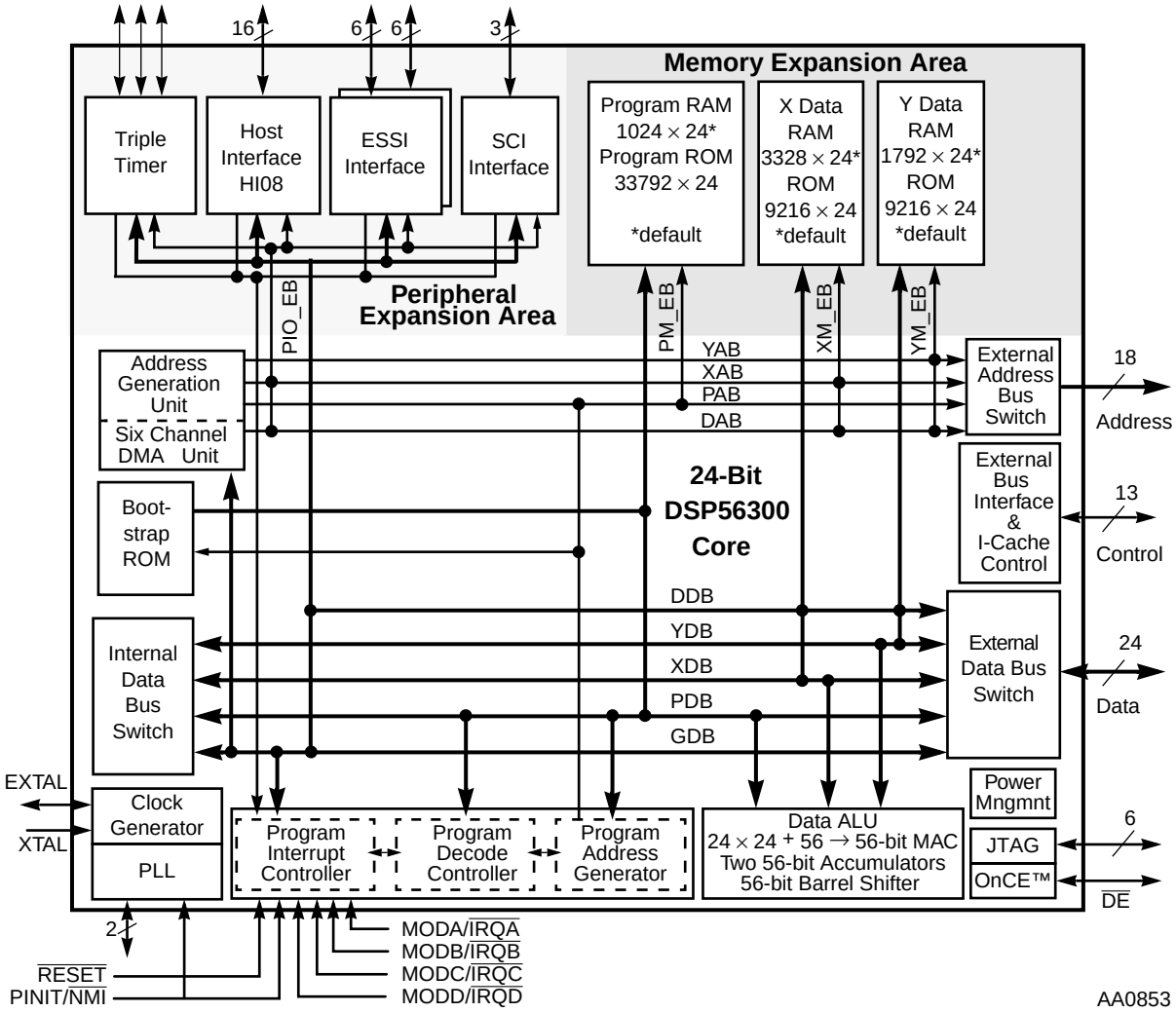

Figure 1 DSP56304 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56304 FEATURES

- High performance DSP56300 core
  - 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock
  - Object code compatible with the DSP56000 core
  - Highly parallel instruction set
  - Fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC)
  - 56-bit parallel barrel shifter
  - 24-bit or 16-bit arithmetic support under software control
  - Position independent code support
  - Addressing modes optimized for DSP applications
  - On-chip instruction cache controller
  - On-chip memory-expandable hardware stack
  - Nested hardware DO loops
  - Fast auto-return interrupts
  - On-chip concurrent six-channel DMA controller
  - On-chip Phase Lock Loop (PLL) and clock generator
  - On-Chip Emulation (OnCE™) module
  - JTAG Test Access Port (TAP)
  - Address Tracing mode reflects internal accesses at the external port
- On-chip memories
  - Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable:

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data Ram Size
disabled	disabled	1024 × 24-bit	0	3328 × 24-bit	1792 × 24-bit
enabled	disabled	0	1024 × 24-bit	3328 × 24-bit	1792 × 24-bit
disabled	enabled	3584 × 24-bit	0	2048 × 24-bit	512 × 24-bit
enabled	enabled	2560 × 24-bit	1024 × 24-bit	2048 × 24-bit	512 × 24-bit

  - 33, 792 × 24-bit Program ROM with Patch mode update capability using instruction cache memory space
  - 9,216 × 24-bit X data ROM and 9,216 × 24-bit Y data ROM
  - 192 × 24-bit bootstrap ROM

- Off-chip memory expansion
  - Data memory expansion to two 256 K × 24-bit word memory spaces
  - Program memory expansion to one 256 K × 24-bit word memory space
  - External memory expansion port
  - Chip select logic requires no additional circuitry to interface to SRAMs and SSRAMs
  - On-chip DRAM controller requires no additional circuitry to interface to DRAMs
- On-chip peripherals
  - 8-bit parallel Host Interface (HI08), ISA-compatible bus interface, providing a cost-effective solution for applications not requiring the PCI bus
  - Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1)
  - Serial Communications Interface (SCI) with baud rate generator
  - Triple timer module
  - Up to thirty-four programmable General Purpose I/O pins (GPIO), depending on which peripherals are enabled
- Reduced power dissipation
  - Very low power CMOS design
  - Wait and Stop low power standby modes
  - Fully-static logic, operation frequency down to DC
  - Optimized power management circuitry

TARGET APPLICATIONS

The DSP56304 is intended for use in embedded multifunction DSP applications requiring large on-board ROM spaces, such as wireless products that combine standard cellular phone operation with options such as two-way digital paging and fax capability in one unit.

PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56304 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

Table 1 DSP56304 Documentation

Document Name	Description of Contents	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56304 User's Manual	Detailed description of DSP56304 memory, peripherals, and interfaces	DSP56304UM/AD
DSP56304 Technical Data	DSP56304 pin and package descriptions, and electrical and timing specifications	DSP56304/D

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