DSP56301

Product Brief
24-bit Digital Signal Processor

The DSP56301, is the first member in the new DSP56300 Family. This family uses a high performance, single clock cycle per instruction engine providing two fold performance increase over Motorola's popular DSP56000 Family, while retaining code compatibility. Several significant architectural enhancements include a barrel shifter, 24 bit addressing, instruction cache and DMA functionality.

The DSP56301 offers 66/80 MIPS using an internal 66/80 MHz clock at 3.0-3.6 volts. The DSP56300 family offers a new level of performance in MIPS, rich instruction set and low power dissipation enabling a new generation of products in wireless, telecommunications, and multimedia.

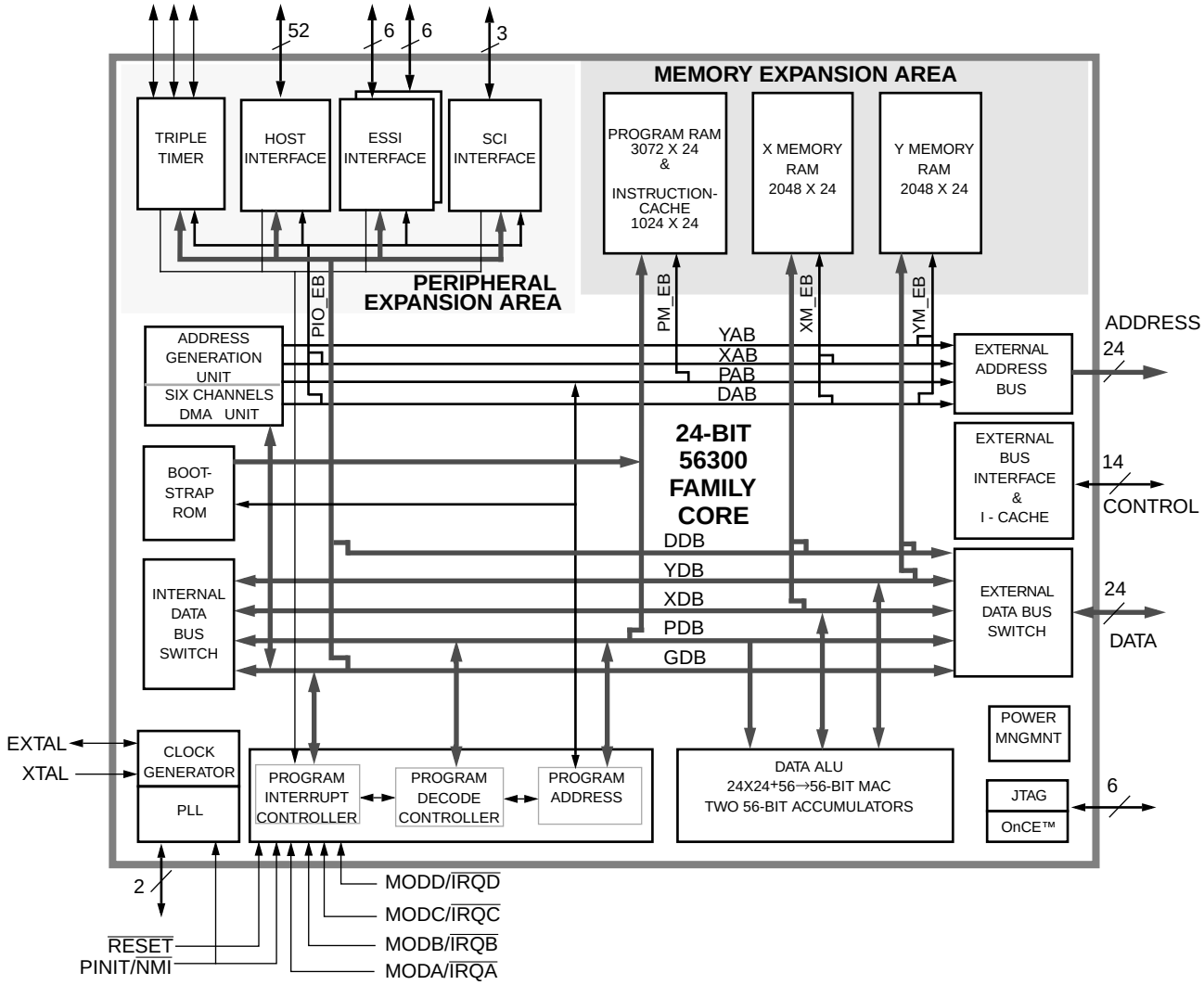

Figure 1 DSP56301 Block Diagram

DSP56301 Features

DSP56300 Family Core

- 66/80 MIPS with a 66/80 MHz internal clock at 3.0-3.6 volts
- Single clock per instruction execution
- Code compatible with DSP56000 family
- Fully-static logic with operation to DC
- Wait, stop and intelligent power control circuitry powers down unused memories, peripherals and core logic on each individual instruction.
- OnCE with added JTAG support for system debugging and testing
- On-chip PLL

ALU Enhancements over DSP56000

- Fully pipelined barrel shifter supports bit stream parsing and generation
- Conditional ALU instruction
- 16 bit arithmetic supports cellular and videotelephony standards

Address Generation Unit Enhancements over DSP56000

- 24 bit addressing provides 16M word addressing for Program, X and Y memories
- Program Counter relative addressing improves operating system and compiler efficiency
- Immediate offset addressing

Program Controller Enhancements over DSP56000

- Hard stack extension in data memory allows unlimited stack depth without programmer overhead
- Support for Instruction Cache

Direct Memory Access Unit

- 6 channel fully concurrent DMA supports 120 Mbyte/sec transfers at 80 MHz
- Dedicated address and data buses support concurrent memory accesses
- Supports peripheral interrupts, internal and external memory reads/writes

DSP56301 Peripherals/External Buses

- Modular peripheral and memory design
- Glueless interface to PCI, ISA, and other DSP56301 buses
- One Serial Communication Interface module
- Two Enhanced Serial Synchronous Interface modules
- Three independent Timer modules
- Glueless interface to SRAM, Synchronous SRAM, DRAM and memory mapped peripherals.
- Off-chip expansion to 2^{24} words for program, X and Y memory

DSP56301 On-chip memories

- On-Chip 2048 × 24 Bit X Data RAM
- On-Chip 2048 × 24 Bit Y Data RAM
- On-Chip 3072 × 24 Bit Program RAM
- On-Chip 1024 × 24 Bit Instruction Cache/Program RAM
- On-Chip 192 × 24 Bit Bootstrap ROM

Documentation

The three documents listed in Table 1 are required for a complete description of the DSP56301 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center listed on the back page.

Table 1 DSP56301 Documentation

Topic	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FAM/AD
DSP56301 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56301UM/AD
DSP56301 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56301/D

Literature Distribution Centers
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036 USA
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbor Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.