# DSP56167

## *Advance Information*
## 16-BIT DIGITAL SIGNAL PROCESSOR

The general purpose, programmable DSP56167 is an enhanced version of the DSP56166 with added features. Designed primarily for speech coding and digital communications, the DSP56167 has a built-in ΣΔ codec and Phase Lock Loop (PLL). This MPU-style DSP also contains memories and digital peripherals that provide a cost effective, high performance solution to many DSP applications. On-Chip Emulation (OnCE™) circuitry provides convenient and inexpensive debug facilities normally available only through expensive external hardware. This RAM-based DSP contains a 2 K × 16 Program RAM and a 4 K × 16 data RAM. The Central Processing Unit (CPU) consists of three execution units operating in parallel, allowing up to six operations to occur in an instruction cycle. This parallelism greatly increases the effective processing speed of the DSP56167. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The DSP56167 is a member of Motorola's DSP56100 family of 16-bit Digital Signal Processors (DSPs).

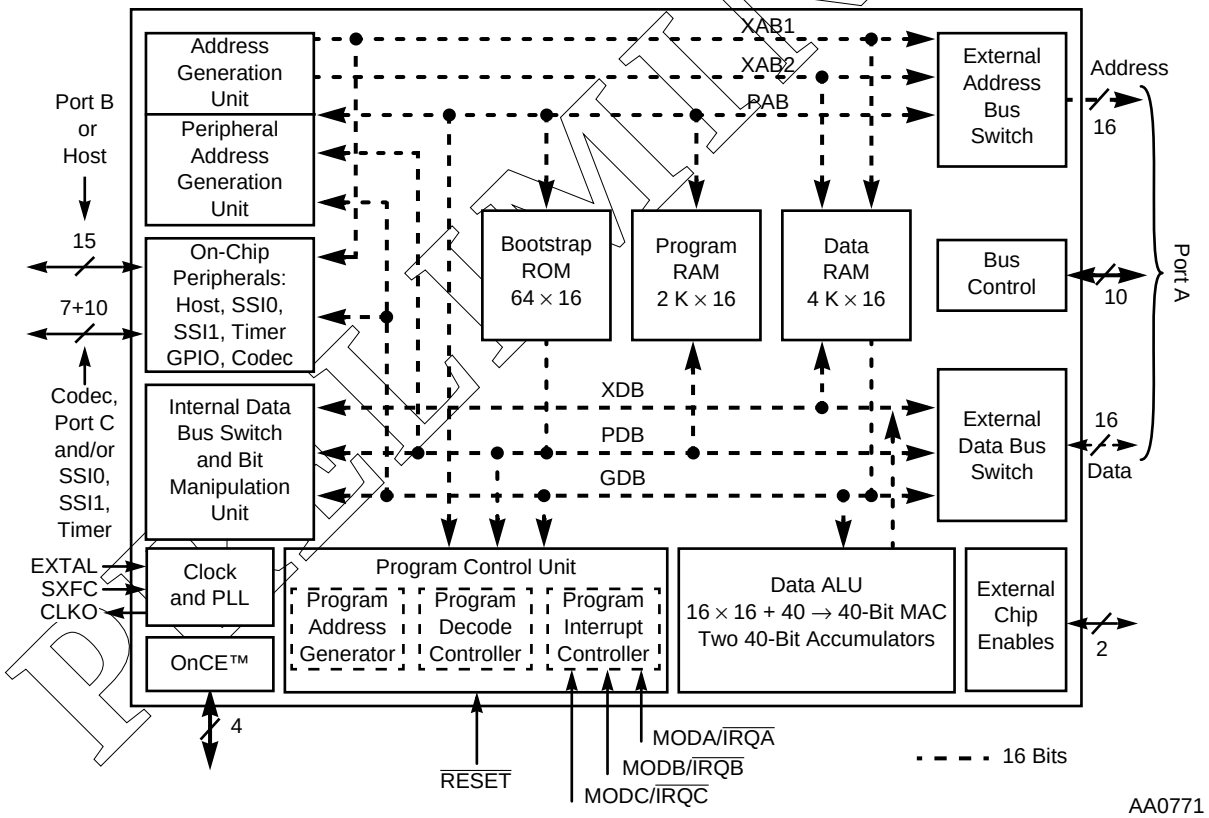


**Figure 1** DSP56167 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without

# DSP56167 FEATURES

- Digital Signal Processing Core
  - Up to 30 Million Instructions Per Second (MIPS) at 60 MHz with 33.3 ns instruction cycle
  - Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
  - 2 × 40-bit accumulators with extension byte
  - Fractional and integer arithmetic with support for multiprecision arithmetic
  - Highly parallel instruction set with unique DSP addressing modes
  - Nested hardware DO loops including infinite loops and DO zero loop
  - Two instruction LMS adaptive filter loop
  - Fast auto-return interrupts
  - Three external interrupt request pins
  - Three 16-bit internal data and three 16-bit internal address buses
  - Individual programmable wait states on the external bus for program, data, and peripheral memory spaces
  - Programmable absolute short addressing mode
  - Off-chip memory-mapped peripheral space with programmable access time and separate peripheral enable pin
  - Peripheral Address Generation Unit (PAGU)
  - On-chip memory-mapped peripheral registers
  - On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging with $\overline{DR}$ line static latch with Reset
- Memory
  - Modified Harvard architecture permits simultaneous accesses to program and data memories
  - 2 K × 16-bit on-chip Program RAM
  - 4 K × 16-bit on-chip data RAM
  - 64 × 16-bit bootstrap ROM
  - External memory expansion with 16-bit address and data buses with static latches with Reset and software-controlled $\overline{BG}$ pull-down
  - Bootstrap loading from external byte-wide Program ROM, Host Interface, or 16-bit Synchronous Serial Interface (SSI0)

- Peripherals
  - Up to twenty-five General Purpose Input / Output (GPIO) pins, depending on which peripherals are enabled
  - Byte-wide Host Interface with Direct Memory Access (DMA) support (or up to fifteen Port B GPIO lines)
  - On-chip ΣΔ voice band codec, Analog-to-Digital (A / D) and Digital-to-Analog (D / A)
    - Internal voltage reference (1 / 2 of positive power supply) and split-voltage operation (with respect to the core)
    - No off-chip components required
  - 16-bit SSI support: two 4-pin ports (or up to eight Port C GPIO lines)
  - One 16-bit timer / event counter (or two Port C GPIO lines)
  - Double-buffered peripherals
  - Independent external chip enables $\overline{BR}$ and $\overline{PEREN}$ during Bus Master mode
  - Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock with a wide input frequency range (12.2 KHz to 60 MHz) that initializes to a preset low frequency operation during hardware reset
- Energy Efficient Design
  - Power-saving Wait and Stop modes
  - Fully static, HCMOS design allows operation from 60 MHz down to DC operating frequencies
  - 112-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package

## PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56167 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW) (the source for the latest information)

**Table 1** DSP56167 Documentation

| Name | Description | Order Number |
|---|---|---|
| DSP56100 Family Manual | Detailed description of the DSP56100 family processor core and instruction set | DSP56100FM / AD |
| DSP56167 User's Manual | Detailed functional description of the DSP56167 memory configuration, operation, and register programming | See note below |
| DSP56167 Technical Data | DSP56167 features list and physical, electrical, timing, and package specifications | DSP56167 / D |

Note: The DSP56167 User's Manual is currently being developed and will not be available for general release until the end of the fourth quarter of 1996. The DSP56167 is a feature expanded, enhanced version of the DSP56166 and is entirely software compatible. Until the DSP56167 User's Manual is available, the user can refer to the *DSP56166 User's Manual*, order number DSP56166UM / AD for information common to both chips and **Section 4** of the DSP56167 Technical Data sheet, order number DSP56167 / D, for a description of the added features and enhanced capability of the DSP56167.





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