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PRODUCT INFORMATION

DSP56009

Product Brief

24-Bit Digital Signal Processor

The DSP56009 is a high performance, programmable Digital Signal Processor (DSP) suitable for a variety of digital audio decompression functions, such as Dolby AC-3® Surround, MPEG1 Layer 2, and Digital Theater Systems™ (DTS) which require the large memory provided by this DSP. The DSP56009 is an MPU-style general purpose DSP, composed of the same, efficient, 24-bit digital signal processor core used by other members of the Motorola 56000-Family DSPs, large program and data memories required by the most advanced signal processing algorithms, various peripherals optimized for audio, and support circuitry. The memory and peripherals differentiate this DSP from the other family members. Figure 1 shows the DSP core, which is fed by a large program ROM, two independent data RAMs, two data ROMs, a Serial Audio Interface, Serial Host Interface, External Memory Interface, dedicated I/O lines, on-chip Phase-Locked Loop (PLL), and On-Chip Emulation (OnCE™) port.

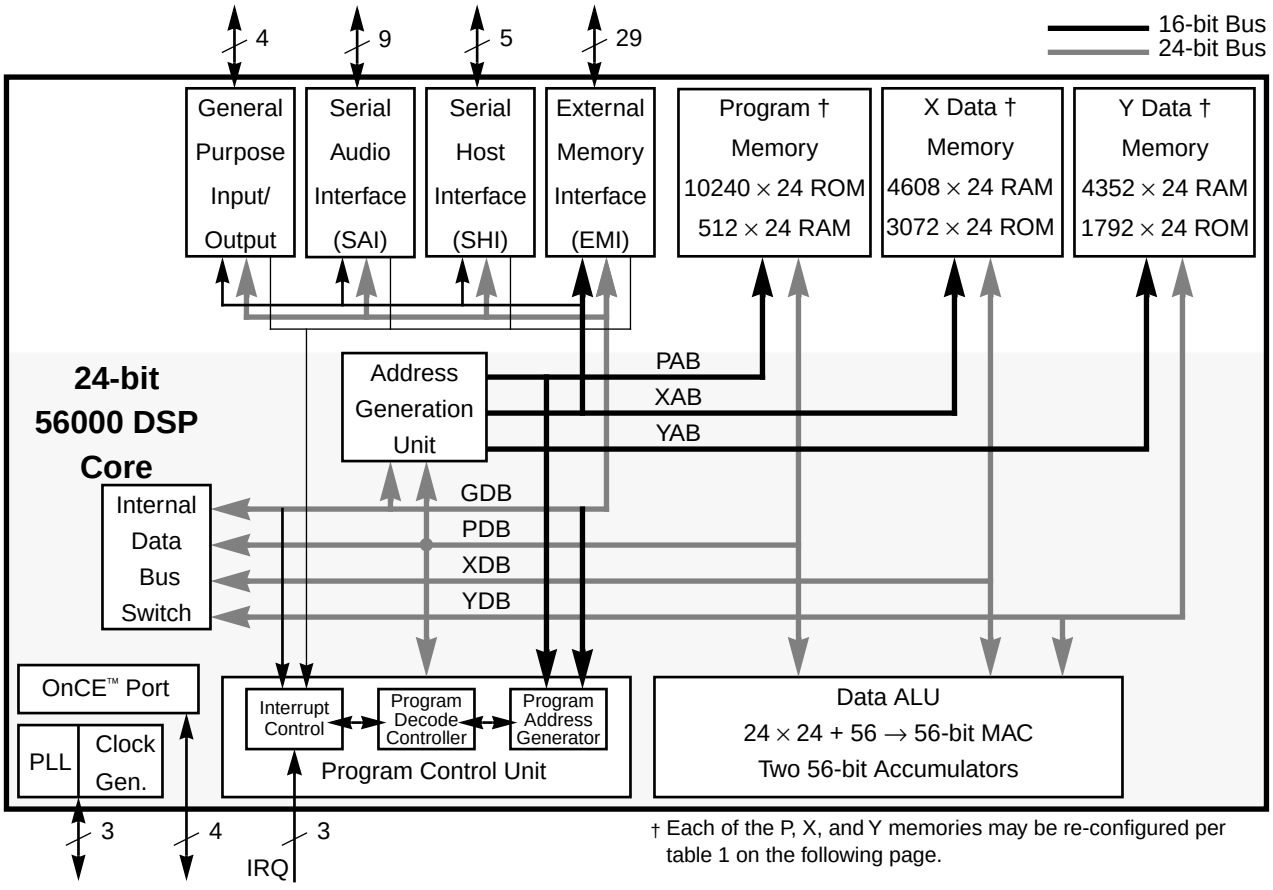

Figure 1 DSP56009 Block Diagram

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DSP56009 Features

Digital Signal Processing Core

- Efficient, object-code compatible, 24-bit 56000-Family DSP engine
  - — Initially 40 Million Instructions Per Second (MIPS) – 25 ns instruction cycle at 80 MHz
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 56-bit accumulators including extension byte
  - — Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
  - — 56-bit addition / subtraction in one instruction cycle
  - — Fractional and integer arithmetic with support for multi-precision arithmetic
  - — Hardware support for block-floating point Fast Fourier Transforms (FFT)
  - — Hardware nested DO loops
  - — Zero-overhead fast interrupts (two instruction cycles)
  - — PLL based clocking with a wide range of frequency multiplications (1 to 4096) and power saving clock divider (2^i : i = 0 to 15). Reduces clock noise
  - — Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories

Memory

Table 1 lists the memory configurations of the DSP56009.

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 10240 × 24-bit on-chip program ROM*
- 4608 × 24-bit on-chip X-data RAM and 3072 × 24-bit on-chip X-data ROM*
- 4352 × 24-bit on-chip Y-data RAM and 1792 × 24-bit on-chip Y-data ROM*
- 512 × 24-bit on-chip Program RAM and 64 × 24-bit bootstrap ROM
- Up to 2304 × 24-bit from X and Y data RAM can be switched to Program RAM giving a total of 2816 × 24-bits of Program RAM
- Bootstrap loading from Serial Host Interface or External Memory Interface

Table 1 DSP56009 Internal Memory Configurations

	No Switch (PEA=0, PEB=0)	Switch A (PEA=1, PEB=0)	Switch B (PEA=0, PEB=1)	Switch A+B (PEA=1, PEB=1)
P: RAM	0.5K	1.25K	2.0K	2.75K
X: RAM	4.5K	3.75K	3.75K	3.0K
Y: RAM	4.25K	4.25K	3.5K	3.5K
P: ROM	10.0K	10.0K	10.0K	10.0K
X: ROM	3.0K	3.0K	3.0K	3.0K
Y: ROM	1.75K	1.75K	1.75K	1.75K

*These ROMs may be factory programmed with data / program provided by the application developer.

Peripheral and Support Circuits

- Serial Audio Interface (SAI) includes two receivers and three transmitters, master or slave capability, and implementation of I^2S, Sony, and Matshushita audio protocols; two sets of SAI interrupt vectors
- Serial Host Interface (SHI) features single master capability, 10-word receive FIFO, and support for 8-, 16- and 24-bit words
- External Memory Interface (EMI), implemented as a peripheral supporting:
  - Page-mode DRAMs (one or two chips): 64k × 4, 256k × 4, and 4M × 4 bits
  - SRAMs (one to four): 256k × 8 bits
  - Data bus may be 4 or 8 bits wide
  - Data words may be 8, 12, 16, 20, or 24 bits wide
- Four dedicated, independent, programmable General Purpose I/O (GPIO) lines
- On-chip peripheral registers memory mapped in data memory space
- Three external interrupt request pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software programmable, Phase-Locked Loop (PLL) based frequency synthesizer for the core clock
- Power saving wait and stop modes
- Fully static, HCMOS design for operating frequencies from 80 MHz down to DC
- 80-pin plastic Quad Flat Pack surface-mount package; 14 × 14 × 2.45 mm; 0.65 mm lead pitch
- Completely pin compatible with the DSP56004 and DSP56007 for easy upgrades
- 5V power supply

Documentation

The three documents listed in Table 2 are required for a complete description of the DSP56009 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center listed below.

Table 2 Additional DSP56009 Documentation

Document Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56009 User's Manual	Detailed description of memory, peripherals, and interfaces	N/A
DSP56009 Data Sheet	Electrical and timing specifications, and pin and package descriptions	N/A

Literature Distribution Centers
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona USA 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbor Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.