

# DSP56005

## Product Brief 24-bit Digital Signal Processor

The DSP56005 is an MPU-style general purpose Digital Signal Processor (DSP), composed of an efficient 24-bit digital signal processor core, program and data memories, various peripherals, and support circuitry. The 56000-Family-compatible DSP core is fed by a large program RAM, two independent data RAMs, and two data ROMs with sine and arc-tangent tables. Like the DSP56002, the DSP56005 contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), parallel Host Interface (HI), a 24-bit timer / event counter, and On-Chip Emulation (OnCE™) port. Unique features of the DSP56005 include the large on-chip program memory, five Pulse Width Modulators (PWM), a watchdog timer, and an address decode pin for external peripherals. This combination of features, illustrated in Figure 1, makes the DSP56005 a cost-effective, high-performance solution for many DSP and control applications, especially in high-performance motor control, optical disk drives and audio processing.

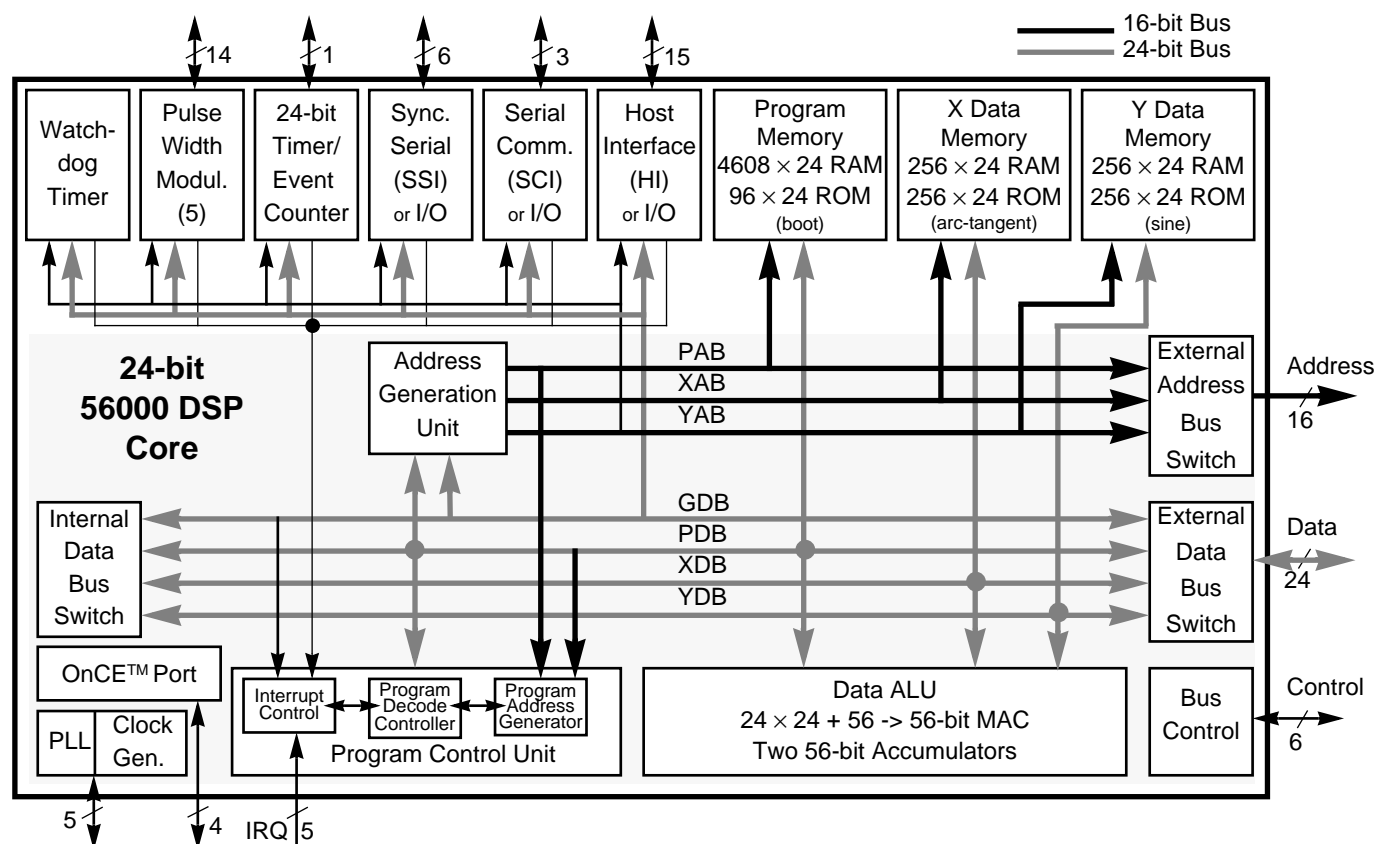


Figure 1 DSP56005 Block Diagram

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# DSP56005 Features

## Digital Signal Processing Core

- Efficient, object code compatible, 24-bit 56000-Family DSP engine
  - Up to 25 Million Instructions per Second (MIPS) – 40 ns instruction cycle at 50 MHz
  - Up to 150 Million Operations per Second (MOPS) at 50 MHz
  - Highly parallel instruction set with unique DSP addressing modes
  - Two 56-bit accumulators including extension byte
  - Parallel  $24 \times 24$ -bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - Double precision  $48 \times 48$ -bit multiply with 96-bit result in 6 instruction cycles
  - 56-bit Addition/subtraction in 1 instruction cycle
  - Fractional arithmetic with support for multiprecision arithmetic
  - Hardware support for block-floating point FFT
  - Hardware nested DO loops
  - Zero-overhead fast interrupts (2 instruction cycles)
  - Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories

## Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- $4608 \times 24$ -bit on-chip program RAM and  $96 \times 24$ -bit bootstrap ROM
- Two  $256 \times 24$ -bit on-chip data RAMs
- Two  $256 \times 24$ -bit on-chip data ROMs containing sine and arc-tangent tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

## Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with Direct Memory Access (DMA) support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
- Serial Communication Interface (SCI) for full-duplex asynchronous communications
- Five Pulse Width Modulators (PWM)
  - Three with alternate outputs; two with open drain or TTL outputs
  - 9- to 16-bit data width
  - Alternate outputs independently selectable as active-high or active-low
- 24-bit timer/event counter also generates and measures digital waveforms
- 16-bit Watchdog timer
- On-chip peripheral registers memory mapped in data memory space
- Double buffered peripherals
- Up to 25 general purpose I/O pins
- Five external interrupt request pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase-Locked Loop (PLL) based frequency synthesizer for the core clock
- External peripheral address decode signal
- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 50 MHz down to DC
- 144-pin Thin Quad Flat Pack (TQFP) surface-mount package;  $20 \times 20 \times 1.4$  mm
- 5 V Power supply


## Documentation

More detailed documentation is available describing the DSP56005. The three documents listed in are required for a complete description of the DSP56005 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor or semiconductor sales office, or through a Motorola Literature Distribution Center.

**Table 1** Additional DSP56005 Documentation

Document Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56005 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56003UM/AD
DSP56005 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56005/D

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