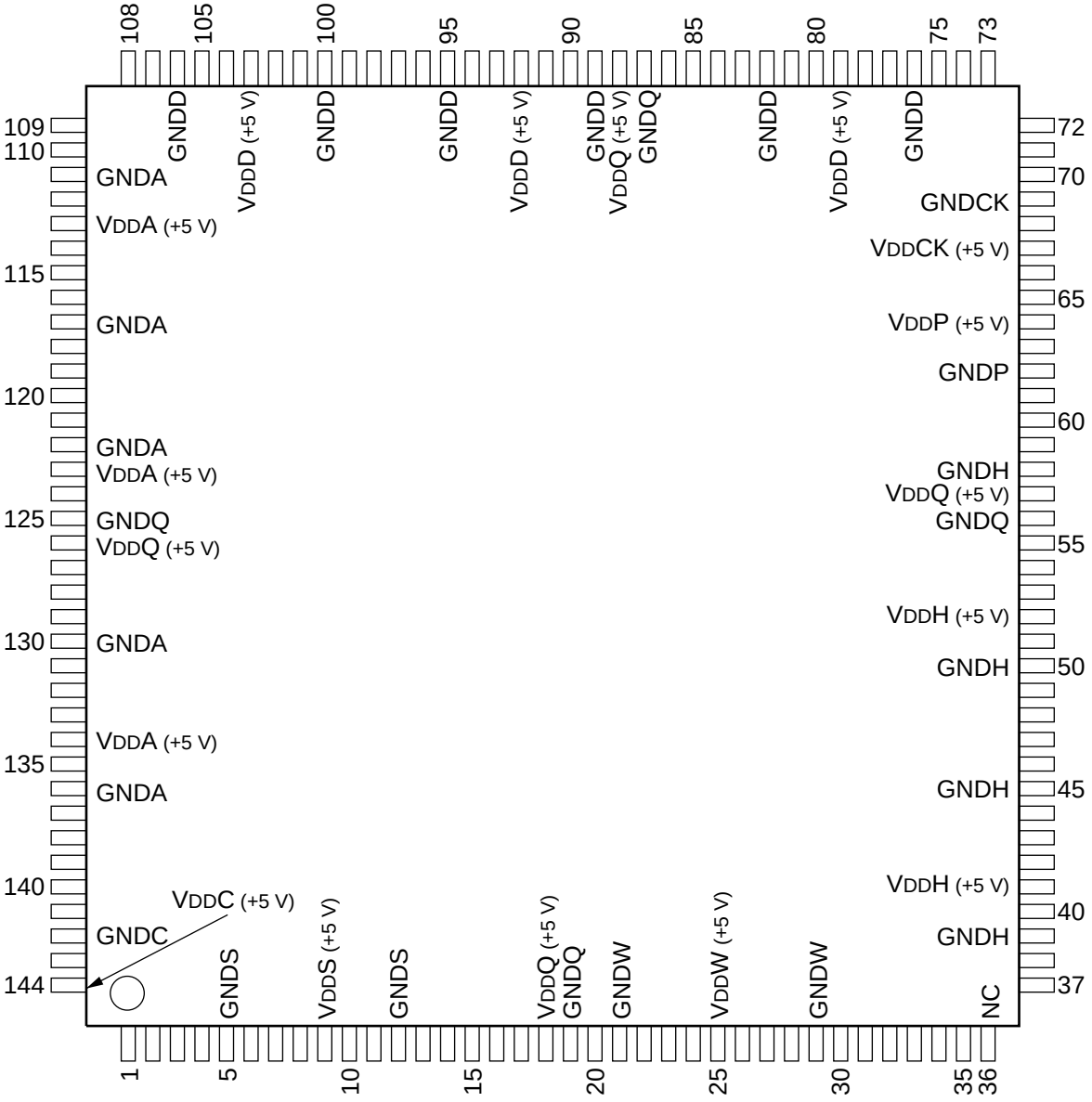
C-MOS 24-BIT DIGITAL SIGNAL PROCESSOR

- TOP VIEW -



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	$\overline{WR}$	37	I/O	H0/PB0	73	I	$\overline{IRQD}$	109	O	A15
2	O	$\overline{RD}$	38	I/O	H1/PB1	74	I/O	D23	110	O	A14
3	I	SRD/PC7	39	—	GNDH	75	I/O	D22	111	—	GNDA
4	I/O	SC1/PC4	40	I/O	H2/PB2	76	—	GNDD	112	O	A13
5	—	GNDS	41	—	V_{DD}H	77	I/O	D21	113	—	V_{DD}A
6	O	STD/PC8	42	I/O	H3/PB3	78	I/O	D20	114	O	A12
7	I/O	SC2/PC5	43	I/O	H4/PB4	79	—	V_{DD}D	115	O	A11
8	I/O	SCK/PC6	44	I/O	H5/PB5	80	I/O	D19	116	O	A10
9	—	V_{DD}S	45	—	GNDH	81	I/O	D18	117	—	GNDA
10	I/O	SC0/PC3	46	I/O	H6/PB6	82	—	GNDD	118	O	A9
11	O	TXD/PC1	47	I/O	H7/PB7	83	I/O	D17	119	O	A8
12	—	GNDS	48	O	$\overline{HREQ}$/PB13	84	I/O	D16	120	O	A7
13	I	RXD/PC0	49	I	HR/$\overline{W}$/PB11	85	I/O	D15	121	O	A6
14	I/O	SCLK/PC2	50	—	GNDH	86	I/O	D14	122	—	GNDA
15	I/O	TIO	51	I	$\overline{HEN}$/PB12	87	—	GNDQ	123	—	V_{DD}A
16	O	PWAP0	52	—	V_{DD}H	88	—	V_{DD}Q	124	O	A5
17	O	PWAN0	53	I	$\overline{HACK}$/PB14	89	—	GNDD	125	—	GNDQ
18	—	V_{DD}Q	54	I	HA0/PB8	90	I/O	D13	126	—	V_{DD}Q
19	—	GNDQ	55	I	HA1/PB9	91	I/O	D12	127	O	A4
20	I	PWAC0	56	—	GNDQ	92	—	V_{DD}D	128	O	A3
21	—	GNDW	57	—	V_{DD}Q	93	I/O	D11	129	O	A2
22	O	PWAP1	58	—	GNDH	94	I/O	D10	130	—	GNDA
23	O	PWAN1	59	I	HA2/PB10	95	—	GNDD	131	O	A1
24	I	PWAC1	60	I	EXTAL	96	I/O	D9	132	O	A0
25	—	V_{DD}W	61	O	XTAL	97	I/O	D8	133	O	$\overline{PS}$
26	O	PWAP2	62	—	GNDP	98	I/O	D7	134	—	V_{DD}A
27	O	PWAN2	63	I	PCAP	99	I/O	D6	135	O	$\overline{DS}$
28	I	PWAC2	64	—	V_{DD}P	100	—	GNDD	136	—	GNDA
29	—	GNDW	65	I	PINIT	101	I/O	D5	137	O	X/$\overline{Y}$
30	I	PWACLK	66	I	$\overline{RESET}$	102	I/O	D4	138	O	$\overline{EXTP}$
31	O	$\overline{PWB0}$	67	—	V_{DD}CK	103	—	V_{DD}D	139	I/O	DSI/OS0
32	O	$\overline{PWB1}$	68	O	CKOUT	104	I/O	D3	140	O	DSO
33	I	PWBC	69	—	GNDCK	105	I/O	D2	141	I	$\overline{DR}$
34	I	PWBCLK	70	I	MODA/$\overline{IRQA}$	106	—	GNDD	142	—	GNDC
35	I	$\overline{IRQC}$	71	I	MODB/$\overline{IRQB}$	107	I/O	D1	143	I/O	DSCK/OS1
36	—	NC	72	I	MODC/$\overline{NMI}$	108	I/O	D0	144	—	V_{DD}C

INPUT

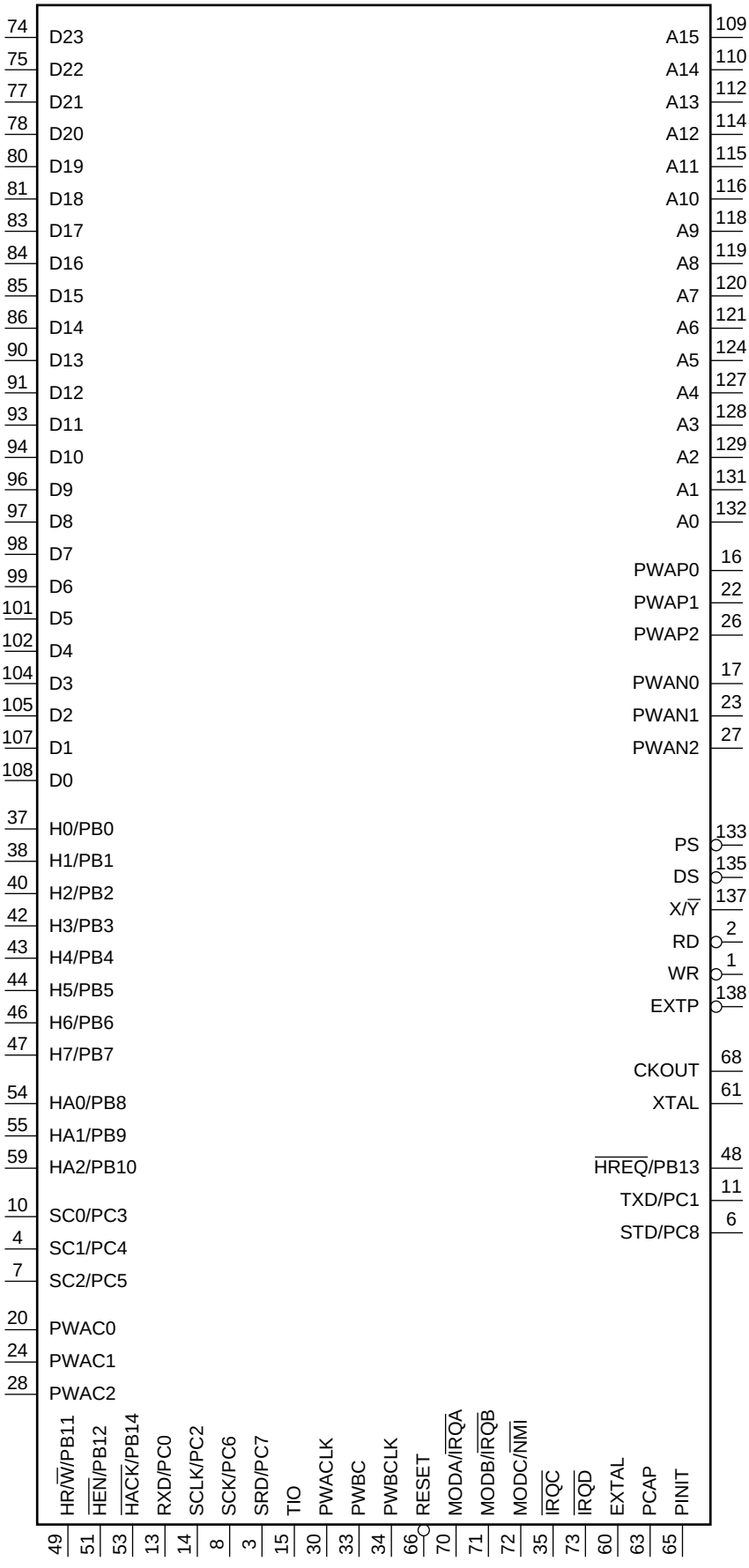
$\overline{DR}$	; DEBUG REQUEST
EXTAL	; EXTERNAL CLOCK/CRYSTAL
HA0 - HA2	; HOST ADDRESS
$\overline{HACK}$	; HOST ACKNOWLEDGE
$\overline{HEN}$	; HOST ENABLE
HR/$\overline{W}$	; HOST READ/WRITE
$\overline{IRQC}$	; EXTERNAL INTERRUPT REQUEST C
$\overline{IRQD}$	; EXTERNAL INTERRUPT REQUEST D
MODA/$\overline{IRQA}$	; MODE SELECT A/EXTERNAL INTERRUPT REQUEST A
MODB/$\overline{IRQB}$	; MODE SELECT B/EXTERNAL INTERRUPT REQUEST B
MODC/$\overline{NMI}$	; MODE SELECT C/NON-MASKABLE INTERRUPT REQUEST
PCAP	; PLL FILTER CAPACITOR
PINIT	; PLL INITIALIZATION
PWAC0 - PWAC2	; PULSE WIDTH MODULATOR A CARRIER
PWACLK	; PULSE WIDTH MODULATOR A CLOCK
PWBC	; PULSE WIDTH MODULATOR B CARRIER
PWBCLK	; PULSE WIDTH MODULATOR B CLOCK
$\overline{RESET}$	; RESET
RXD	; RECEIVE DATA
SRD	; SSI RECEIVE DATA

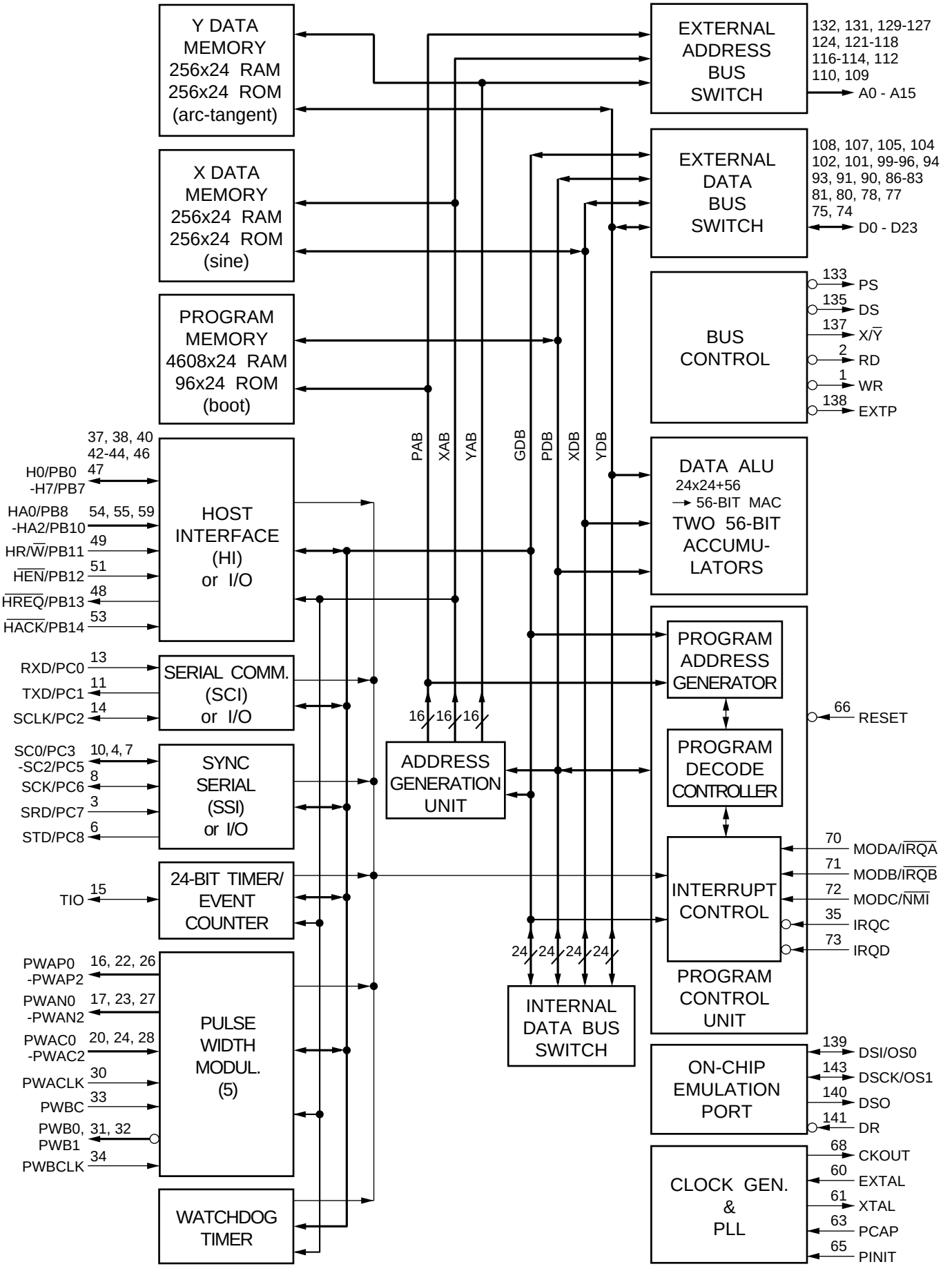
OUTPUT

A0 - A15	; ADDRESS BUS
CKOUT	; OUTPUT CLOCK
$\overline{DS}$	; DATA MEMORY SELECT
$\overline{DSO}$	; DEBUG SERIAL OUTPUT
$\overline{EXTP}$	; EXTERNAL PERIPHERAL
$\overline{HREQ}$	; HOST REQUEST
$\overline{PS}$	; PROGRAM MEMORY SELECT
PWAN0 - PWAN2	; PULSE WIDTH MODULATOR A NEGATIVE
PWAP0 - PWAP2	; PULSE WIDTH MODULATOR A POSITIVE
$\overline{PWB0}$, $\overline{PWB1}$	; PULSE WIDTH MODULATOR B OUTPUT
$\overline{RD}$	; READ ENABLE
STD	; SSI TRANSMIT DATA
TXD	; TRANSMIT DATA
$\overline{WR}$	; WRITE ENABLE
XTAL	; CRYSTAL
X/$\overline{Y}$	; X/$\overline{Y}$ SELECT

INPUT/OUTPUT

D0 - D23	; DATA BUS
DSCK/OS1	; DEBUG SERIAL CLOCK/CHIP STATUS 1
DSI/OS0	; DEBUG SERIAL INPUT/CHIP STATUS 0
H0 - H7	; HOST DATA BUS
SC0 - SC2	; SERIAL CONTROL 0, 1, 2
SCK	; SSI SERIAL CLOCK
SCLK	; SCI SERIAL CLOCK
TIO	; TIMER/EVENT COUNTER INPUT/OUTPUT


74 D23
75 D22
77 D21
78 D20
80 D19
81 D18
83 D17
84 D16
85 D15
86 D14
90 D13
91 D12
93 D11
94 D10
96 D9
97 D8
98 D7
99 D6
101 D5
102 D4
104 D3
105 D2
107 D1
108 D0
37 H0/PB0
38 H1/PB1
40 H2/PB2
42 H3/PB3
43 H4/PB4
44 H5/PB5
46 H6/PB6
47 H7/PB7
54 HA0/PB8
55 HA1/PB9
59 HA2/PB10
10 SC0/PC3
4 SC1/PC4
7 SC2/PC5
20 PWAC0
24 PWAC1
28 PWAC2
109 A15
110 A14
112 A13
114 A12
115 A11
116 A10
118 A9
119 A8
120 A7
121 A6
124 A5
127 A4
128 A3
129 A2
131 A1
132 A0
16 PWAP0
22 PWAP1
26 PWAP2
17 PWAN0
23 PWAN1
27 PWAN2
133 PS
135 DS
137 X/Y
2 RD
1 WR
138 EXTP
68 CKOUT
61 XTAL
48 HREQ/PB13
11 TXD/PC1
6 STD/PC8
49 HR/W/PB11
51 HEN/PB12
53 HACK/PB14
13 RXD/PC0
14 SCLK/PC2
8 SCK/PC6
3 SRD/PC7
15 TIO
30 PWACLK
33 PWBC
34 PWBCLK
66 RESET
70 MODA/IRQA
71 MODB/IRQB
72 MODC/NMI
35 IRQC
73 IRQD
60 EXTAL
63 PCAP
65 PINIT


Y DATA MEMORY 256x24 RAM 256x24 ROM (arc-tangent)
X DATA MEMORY 256x24 RAM 256x24 ROM (sine)
PROGRAM MEMORY 4608x24 RAM 96x24 ROM (boot)
EXTERNAL ADDRESS BUS SWITCH
132, 131, 129-127
124, 121-118
116-114, 112
110, 109
A0 - A15
EXTERNAL DATA BUS SWITCH
108, 107, 105, 104
102, 101, 99-96, 94
93, 91, 90, 86-83
81, 80, 78, 77
75, 74
D0 - D23
BUS CONTROL
133 PS
135 DS
137 X/Y
2 RD
1 WR
138 EXTP
PAB
XAB
YAB
GDB
PDB
XDB
YDB
DATA ALU
24x24+56
→ 56-BIT MAC
TWO 56-BIT ACCUMU-LATORS
37, 38, 40
42-44, 46
H0/PB0 47
-H7/PB7
HA0/PB8 54, 55, 59
-HA2/PB10
HR/W/PB11 49
HEN/PB12 51
HREQ/PB13 48
HACK/PB14 53
HOST INTERFACE (HI) or I/O
RXD/PC0 13
TXD/PC1 11
SCLK/PC2 14
SERIAL COMM. (SCI) or I/O
SC0/PC3 10, 4, 7
-SC2/PC5
SCK/PC6 8
SRD/PC7 3
STD/PC8 6
SYNC SERIAL (SSI) or I/O
TIO 15
24-BIT TIMER/ EVENT COUNTER
PWAP0 16, 22, 26
-PWAP2
PWAN0 17, 23, 27
-PWAN2
PWAC0 20, 24, 28
-PWAC2
PWACLK 30
PWBC 33
PWB0, 31, 32
PWB1
PWBCLK 34
PULSE WIDTH MODUL. (5)
WATCHDOG TIMER
16 16 16
ADDRESS GENERATION UNIT
24 24 24 24
INTERNAL DATA BUS SWITCH
PROGRAM ADDRESS GENERATOR
PROGRAM DECODE CONTROLLER
INTERRUPT CONTROL
PROGRAM CONTROL UNIT
66 RESET
70 MODA/IRQA
71 MODB/IRQB
72 MODC/NMI
35 IRQC
73 IRQD
ON-CHIP EMULATION PORT
139 DSI/OS0
143 DSCK/OS1
140 DSO
141 DR
CLOCK GEN. & PLL
68 CKOUT
60 EXTAL
61 XTAL
63 PCAP
65 PINIT