

SIEMENS

Microcomputer Components

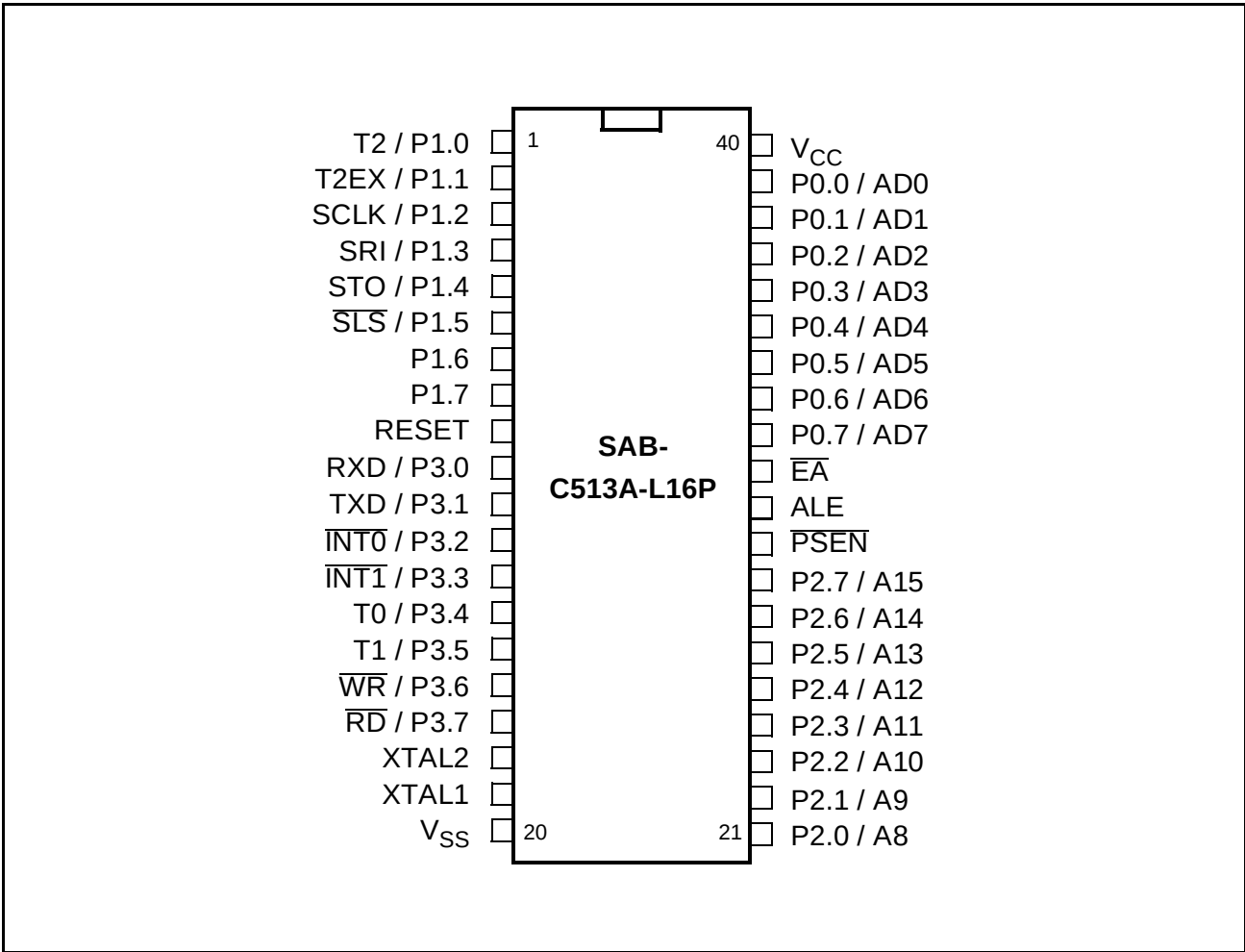
8-Bit CMOS Microcontroller

SAB-C513A-L16P

16 MHz Specification

Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS Microcontroller)
SAB-C513A-L16P	Q67120-C1039	P-DIP-40	for external memory, 16 MHz



Pin Configuration (Top view)

DC Characteristics

$V_{CC} = 4.0 - 5.5V$; $V_{SS} = 0V$; $T_A = 0$ to $+70\text{ }^{\circ}C$

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. ⁸⁾	max.		
Power supply current:					
Active mode, 16 MHz ⁶⁾	I_{CC}	11	14.3	mA	$V_{CC} = 5V$, ⁴⁾
Idle mode, 16 MHz ⁶⁾	I_{CC}	4.3	5.6	mA	$V_{CC} = 5V$, ⁵⁾
Power Down Mode	I_{PD}	—	50	μA	$V_{CC} = 2 \dots 5.5V$ ³⁾

Notes:

- ³⁾ I_{PD} (Power Down Mode) is measured under following conditions:
 $\overline{EA} = \text{Port0} = V_{CC}$; $\text{RESET} = V_{SS}$; $\text{XTAL2} = \text{N.C.}$; $\text{XTAL1} = V_{CC}$; all other pins are disconnected.
- ⁴⁾ I_{CC} (active mode) is measured with:
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5\text{ ns}$, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; $\text{XTAL2} = \text{N.C.}$;
 $\overline{EA} = \text{Port0} = \text{RESET} = V_{CC}$; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- ⁵⁾ I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5\text{ ns}$, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; $\text{XTAL2} = \text{N.C.}$;
 $\text{RESET} = \overline{EA} = V_{SS}$; $\text{Port0} = V_{CC}$; all other pins are disconnected;
- ⁶⁾ $I_{CC \text{ Max}}$ at other frequencies is given by:
Active mode : $I_{CC} = 0.85 \times f_{OSC} + 0.72$
Idle mode : $I_{CC} = 0.34 \times f_{OSC} + 0.15$
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5V$.
- ⁸⁾ The typical I_{CC} values are periodically measured at $T_A = +25\text{ }^{\circ}C$ but not 100% tested.

AC Characteristics

$V_{CC} = 4.0 - 5.5V$; $V_{SS} = 0V$; $T_A = 0 \text{ to } +70^\circ\text{C}$

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock		
				$1/t_{\text{CLCL}} = 3.5 \text{ MHz to } 16 \text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	85	—	$2t_{\text{CLCL}} - 40$	—	ns
Address setup to ALE	t_{AVLL}	33	—	$t_{\text{CLCL}} - 30$	—	ns
Address hold after ALE	t_{LLAX}	28	—	$t_{\text{CLCL}} - 35$	—	ns
ALE low to valid instr in	t_{LLIV}	—	150	—	$4t_{\text{CLCL}} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	38	—	$t_{\text{CLCL}} - 25$	—	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	153	—	$3t_{\text{CLCL}} - 35$	—	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	—	88	—	$3t_{\text{CLCL}} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	—	0	—	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}^{*)}$	—	43	—	$t_{\text{CLCL}} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXAV}}^{*)}$	55	—	$t_{\text{CLCL}} - 8$	—	ns
Address to valid instr in	t_{AVIV}	—	198	—	$5t_{\text{CLCL}} - 115$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	—	0	—	ns

*) Interfacing the C513 microcontroller to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock 1/t _{CLCL} = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	275	—	6t _{CLCL} – 100	—	ns
$\overline{\text{WR}}$ pulse width	t _{WLWH}	275	—	6t _{CLCL} – 100	—	ns
Address hold after ALE	t _{LLAX2}	90	—	2t _{CLCL} – 35	—	ns
$\overline{\text{RD}}$ to valid data in	t _{RLDV}	—	148	—	5t _{CLCL} – 165	ns
Data hold after $\overline{\text{RD}}$	t _{RHDX}	0	—	0	—	ns
Data float after $\overline{\text{RD}}$	t _{RHDZ}	—	55	—	2t _{CLCL} – 70	ns
ALE to valid data in	t _{LLDV}	—	350	—	8t _{CLCL} – 150	ns
Address to valid data in	t _{AVDV}	—	398	—	9t _{CLCL} – 165	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{LLWL}	138	238	3t _{CLCL} – 50	3t _{CLCL} + 50	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{AWWL}	120	—	4t _{CLCL} – 130	—	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t _{WHLH}	23	103	t _{CLCL} – 40	t _{CLCL} + 40	ns
Data valid to $\overline{\text{WR}}$ transition	t _{QVWX}	13	—	t _{CLCL} – 50	—	ns
Data setup before $\overline{\text{WR}}$	t _{QVWH}	288	—	7t _{CLCL} – 150	—	ns
Data hold after $\overline{\text{WR}}$	t _{WHQX}	13	—	t _{CLCL} – 50	—	ns
Address float after $\overline{\text{RD}}$	t _{RLAZ}	—	0	—	0	ns

SSC Interface Characteristics

Parameter	Symbol	Limit Values				Unit
		13.5 MHz Clock		16 MHz Clock		
		min.	max.	min.		
Clock Cycle Time : Master Mode Slave Mode	t_{SCLK}	592	—	500	—	ns
	t_{SCLK}	530	—	450	—	ns
Clock high time	t_{SCH}	230	—	200	—	ns
Clock low time	t_{SCL}	230	—	200	—	ns
Data output delay	t_{D}	—	100	—	100	ns
Data output hold	t_{HO}	0	—	0	—	ns
Data input setup	t_{S}	100	—	80	—	ns
Data input hold	t_{HI}	100	—	80	—	ns
TC bit set delay	t_{DTC}	—	$16 t_{\text{CLCL}}$	—	$16 t_{\text{CLCL}}$	ns

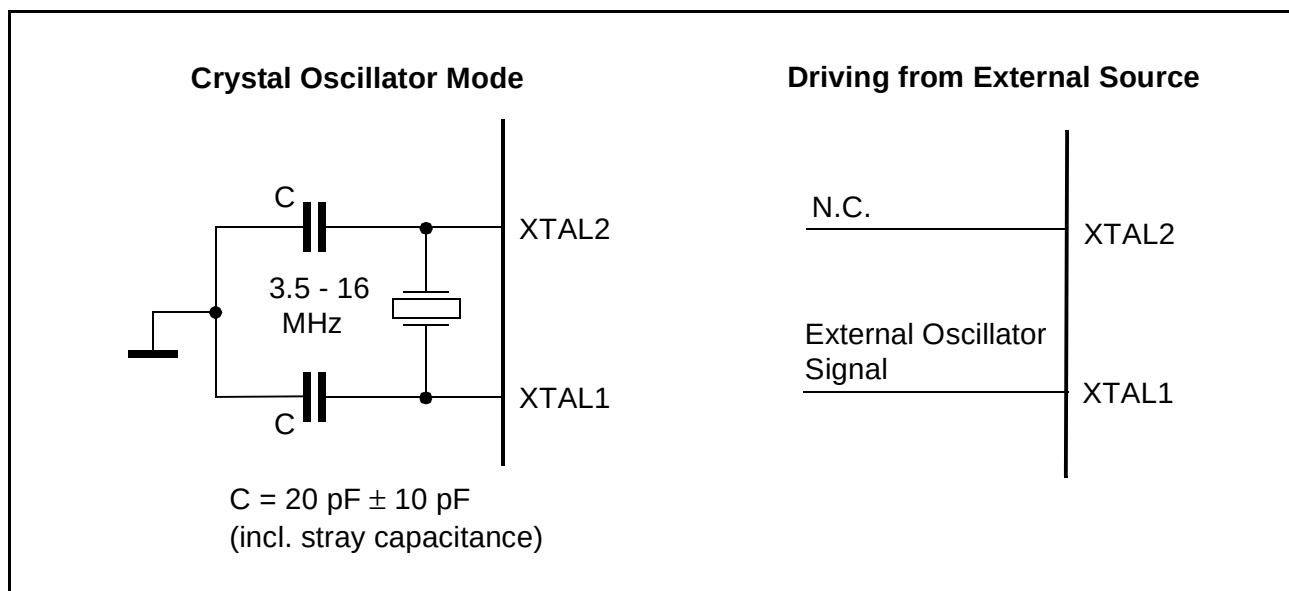
External Clock Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 16 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	62.5	285	ns
High time	t_{CHCX}	15	$t_{\text{CLCL}} - t_{\text{CLCX}}$	ns
Low time	t_{CLCX}	15	$t_{\text{CLCL}} - t_{\text{CHCX}}$	ns
Rise time	t_{CLCH}	—	15	ns
Fall time	t_{CHCL}	—	15	ns

Reset Characteristics

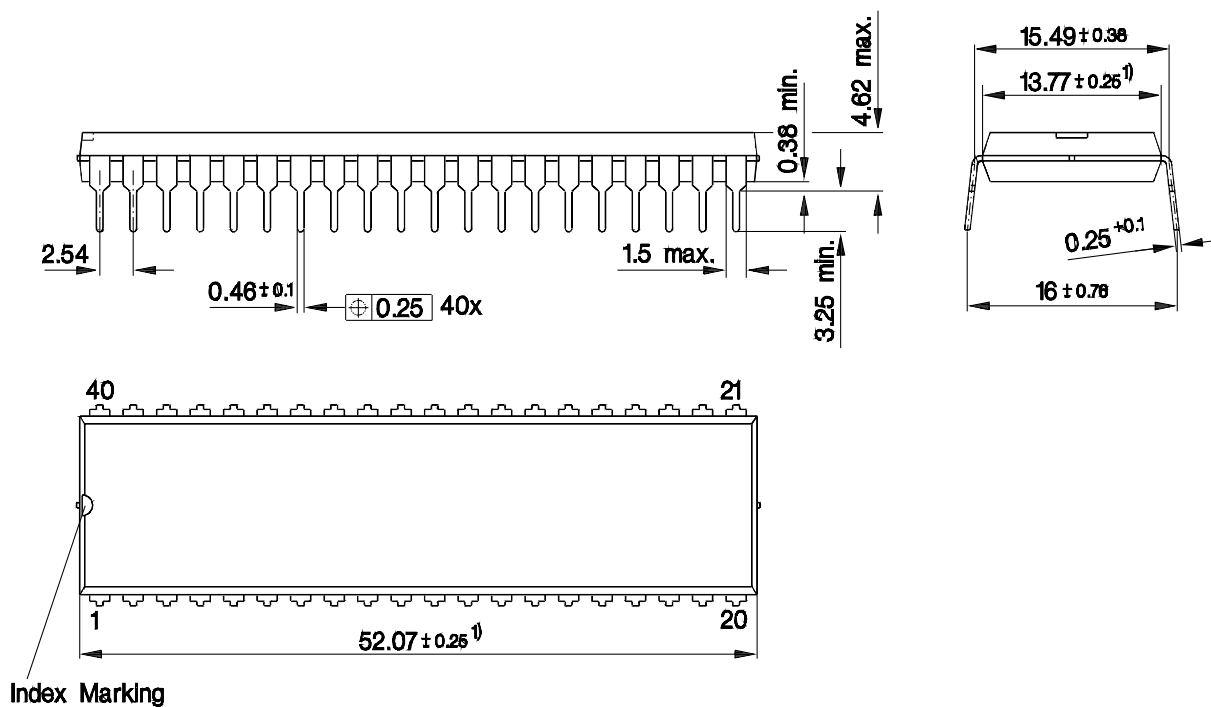
Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock 1/t _{CLCL} = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
RESET high pulse width (when CPU is running)	t _{RES}	1.5	—	24 t _{CLCL}	—	μs

Recommended Oscillator Circuits



Package Outline

Plastic Package, P-DIP-40-2 (Plastic Dual in-Line Package)



¹⁾ Does not include plastic or metal protrusion of 0.25 max. per side