SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C511/C511A
C513/C513A
C513A-H

Data Sheet 06.96

Data Sheet C511/C511A/C513/C513A/C513A-H **Revision History :**	**Current Version : 06.96**
Previous Releases :	02.96, 05.95
Page	Subjects (changes since last revision)
Several 41	Corrections of text Figure 22: external clock configuration corrected

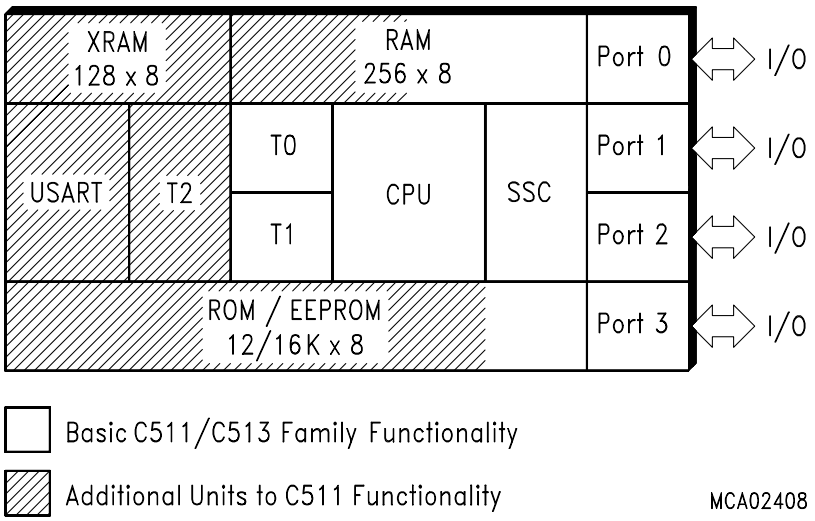
SIEMENS

8-Bit CMOS Microcontroller Family

C511
C511A
C513
C513A
C513A-H

Preliminary

- Fully software compatible to standard 8051/8052 microcontrollers
- Up to 12 MHz operating frequency
- Up to 12 K×8 ROM / EEPROM
- Up to 256×8 RAM
- Up to 256 x 8 XRAM
- Four 8-bit ports
- Up to three 16-bit Timers / Counters (Timer 2 with Up/Down and 16-bit Autoreload Feature)
- Synchronous Serial Channel (SSC)
- Optional USART
- Up to seven interrupt sources, two priority levels
- Power Saving Modes
- P-LCC-44 package (C513A also in P-MQFP-44 package)
- Temperature Ranges : SAB-C511 / 511A / 513 / 513A / C513A-H T_A : 0 ˚C to 70 ˚C
  SAF-C513A T_A : -40 ˚C to 85 ˚C



The C511, C511A, C513, C513A, and C513A-H are members of a family of low cost micro-controllers, which are software compatible with the components of the SAB 8051, SAB 80C51 and C500 families.

The first four versions contains a non-volatile read-only (ROM) program memory. The C513A-H is a version with a 12 Kbyte EEPROM instead of ROM. This device can be used for prototype designs which have a demand for reprogrammable on-chip code memory.

The members of the microcontroller family differ in functionality according **table 1**. They offer different ROM sizes, different RAM/XRAM sizes and a different timer/USART configuration. Common to all devices is an advanced SSC serial port, a second synchronous serial interface, which is compatible to the SPI serial bus industry standard. The functionality of the C513A-H is a superset of all ROM versions of the C511/C513 family.

Table 1
Functionality of the C511/C513 MCUs

Device	ROM Size	EEPROM Size	RAM Size	XRAM Size	Timers [1]	USART	SSC
C511	2.5 KB	–	128 B	–	T0, T1	–	✓
C511A	4 KB	–	256 B	–	T0, T1	–	✓
C513	8 KB	–	256 B	–	T0, T1, T2	✓	✓
C513A	12, 16 KB	–	256 B	256 B	T0, T1, T2	✓	✓
C513A-H	–	12 KB	256 B	256 B	T0, T1, T2	✓	✓

[1] T0/T1 refers to the standard 8051 timer 0/1 units, T2 refers to the 8052 timer 2 unit.

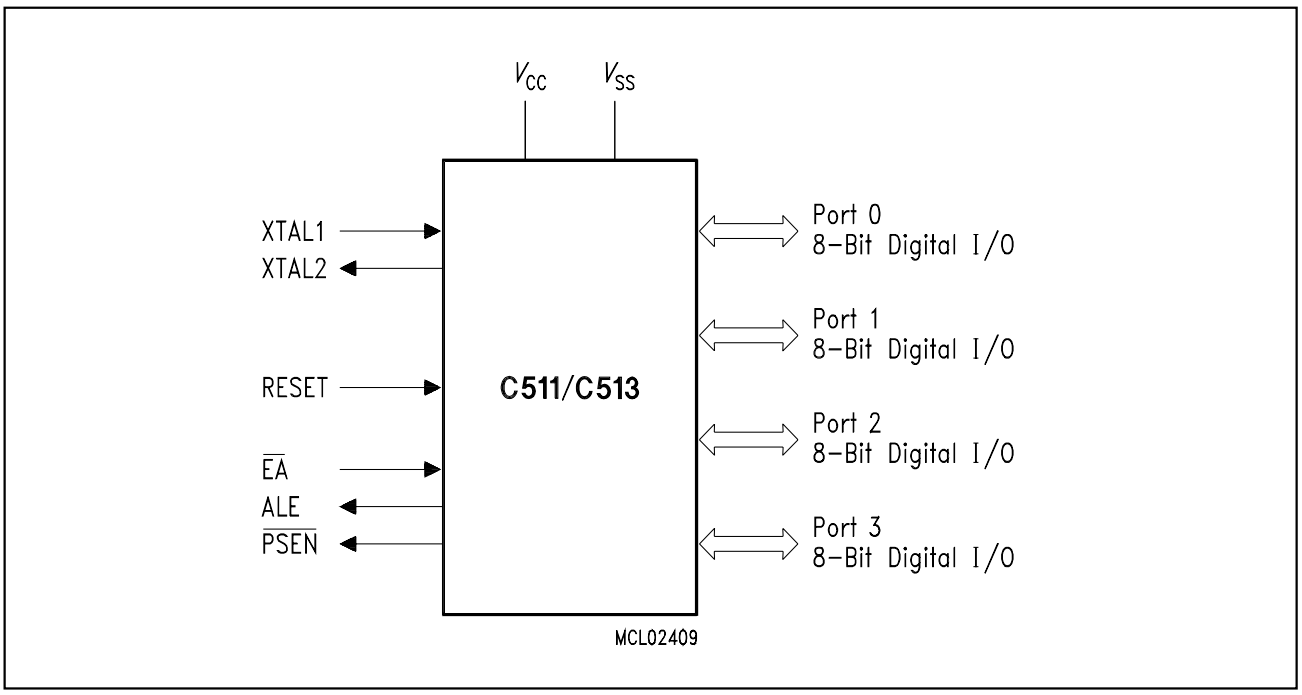


Figure 1
C511/513 Logic Symbol

Table 2
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
C511-RN	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (2.5K), 12 MHz
C511A-RN	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (4K), 12 MHz
C513-1RN	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (8K), 12 MHz
C513A-RN	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (12K), 12 MHz
	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (12K), 12 MHz, ext. temp. – 40 ˚C to 85 ˚C
C513A-2RN	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (16K), 12 MHz
	Q67120-DXXXX	P-LCC-44	with mask-programmable ROM (16K), 12 MHz, ext. temp. – 40 ˚C to 85 ˚C
C513A-2RM	Q67120-DXXXX	P-MQFP-44	with mask-programmable ROM (16K), 12 MHz
	Q67120-DXXXX	P-MQFP-44	with mask-programmable ROM (16K), 12 MHz, ext. temp. – 40 ˚C to 85 ˚C
C513A-LN	Q67120-C1017	P-LCC-44	for external memory (12 MHz)
	Q67120-C1035	P-LCC-44	for external memory (12 MHz), ext. temp. – 40 ˚C to 85 ˚C
C513A-LM	Q67120-C1026	P-MQFP-44	for external memory (12 MHz)
	Q67120-C1036	P-MQFP-44	for external memory (12 MHz), ext. temp. – 40 ˚C to 85 ˚C
C513A-HN	Q67120-C0989	P-LCC-44	with reprogrammable EEPROM (12K), 12 MHz, ext. temp. – 40 ˚C to 85 ˚C

Note : The ordering number of the ROM types (DXXXX extension) is defined after program release (verification) of the customer.

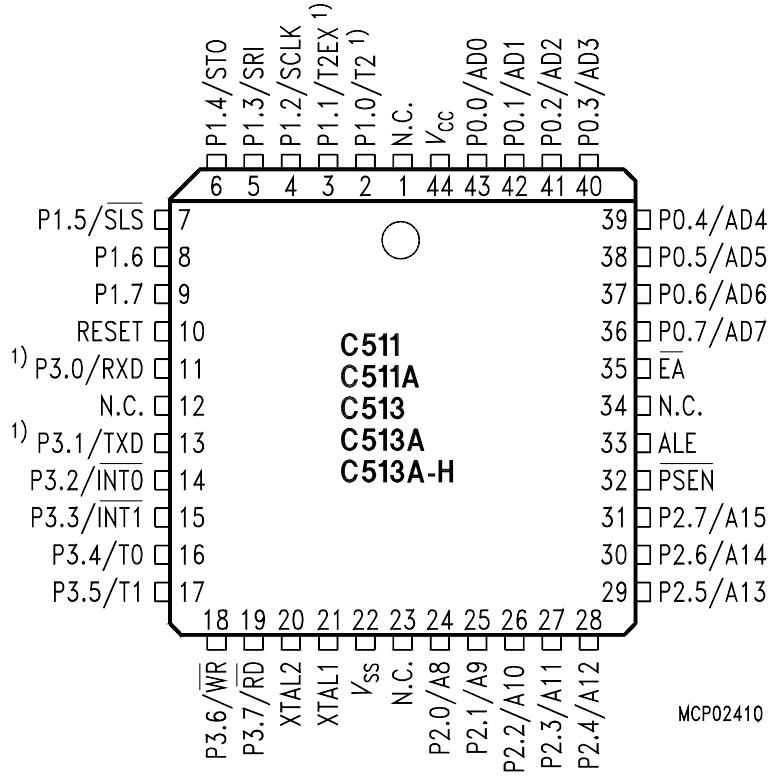


Figure 2
P-LCC-44 Package Pin Configuration (Top View)

If the C513A-H is used in programming mode, the pin configuration is different to **figure 2** and **3** (see **figure 5**).

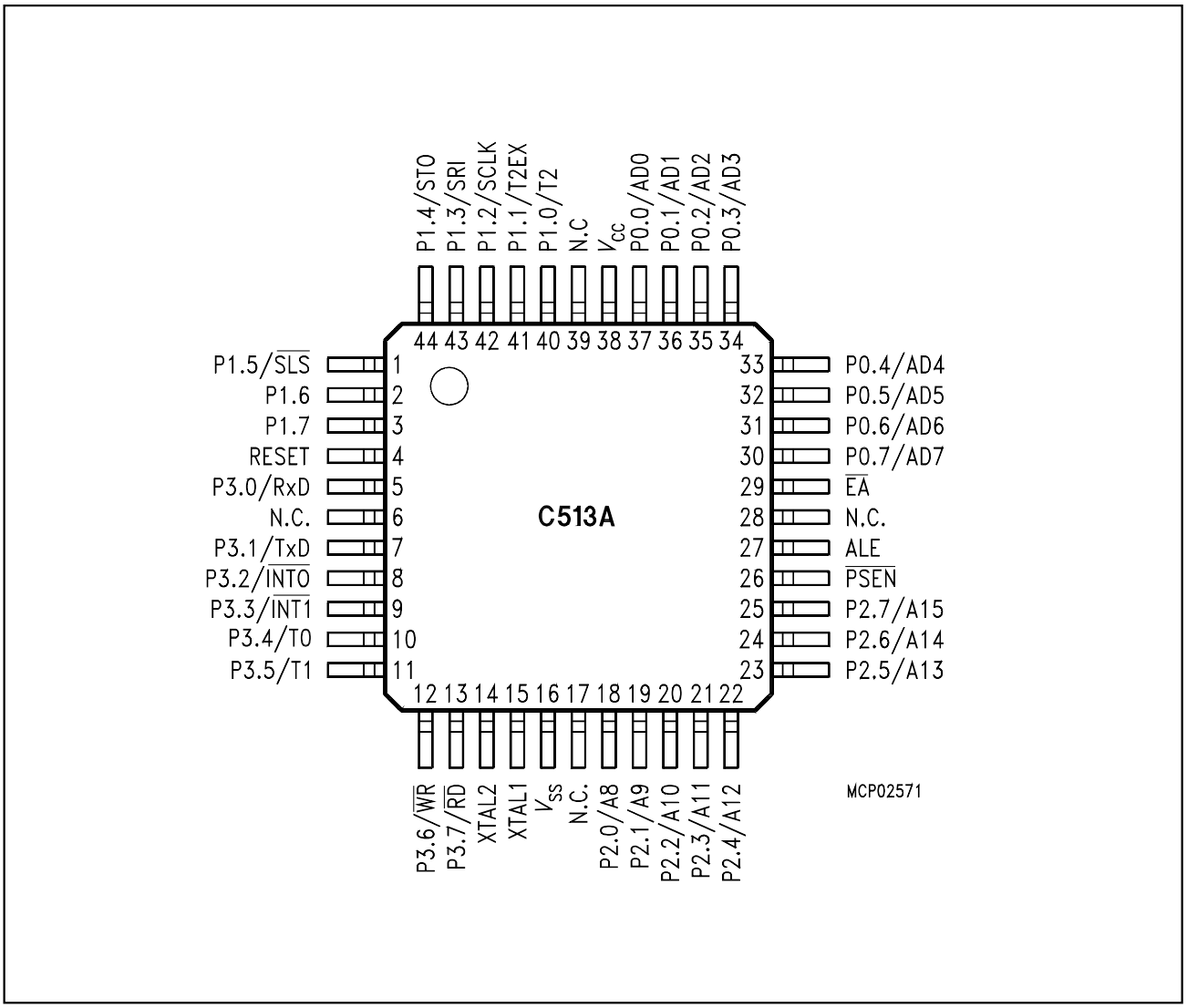


Figure 3
P-MQFP-44 Package Pin Configuration of the C513A (Top View)

Table 3
Pin Definitions and Functions

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-MQFP-44		
P1.7-P1.0	9-2	3-1, 44-40	I/O	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 1 also contains the timer 2 and SSC pins as secondary function. In general the output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. For the outputs of the SSC (SCLK, STO) special circuitry is implemented, providing true push-pull capability. The STO output in addition will have true tristate capability. When used for SSC inputs, the pull-up resistors will be switched off and the inputs will float (high ohmic inputs). The alternate functions are assigned to port 1, as follows: P1.0 T2 Input to counter 2 [1)] P1.1 T2EX Capture -Reload trigger of timer 2 [1)] Up-Down count P1.2 SCLK SSC Master Clock Output SSC Slave Clock Input P1.3 SRI SSC Receive Input P1.4 STO SSC Transmit Output P1.5 $\overline{SLS}$ Slave Select Input [1)] not available in the C511/511A
	2	40		
	3	41		
	4	42		
	5	43		
	6	44		
	7	1		

*) I = Input
O = Output

Table 3
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-MQFP-44		
P3.0-P3.7	11, 13-19	5, 7-13	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3 as follows:
	11	5		P3.0 RXD — Receiver data input (asynchronous) or data input/output (synchronous) of serial interface (USART) [1]
	13	7		P3.1 TXD — Transmitter data output (USART) [1] (asynchronous) or clock output (synchronous) of serial interface
	14	8		P3.2 $\overline{INT0}$ — $\overline{Interrupt\ 0\ input}$ / timer 0 gate control
	15	9		P3.3 $\overline{INT1}$ — $\overline{Interrupt\ 1\ input}$ / timer 1 gate control
	16	10		P3.4 T0 — Counter 0 input
	17	11		P3.5 T1 — Counter 1 input
	18	12		P3.6 $\overline{WR}$ — Write control signal : latches the data byte from port 0 into the external data memory
	19	13		P3.7 $\overline{RD}$ — Read control signal : enables the external data memory to port 0 [1] not available in the C511/511A
XTAL2	20	14	–	**XTAL2** Output of the inverting oscillator amplifier.

*) I = Input
O = Output

Table 3
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-MQFP-44		
XTAL1	21	15	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	24-31	18-25	I/O	**Port 2** is a bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
RESET	10	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

*) I = Input
O = Output

Table 3
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-MQFP-44		
ALE	33	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access. If no external memory is used, the ALE signal generation can be inhibited, reducing system RFI, by clearing register bit EALE in the SYSCON register.
$\overline{EA}$	35	29	I	**$\overline{External\ Access\ Enable}$** When held at high level, instructions are fetched from the internal ROM when the PC is less than the size of the internal ROM : C511 $0A00_H$; C511A 1000_H; C513 2000_H; C513A/A-H 3000_H; C513A-2R 4000_H. When held at low level, the microcontroller fetches all instructions from external program memory.
P0.0-P0.7	43-36	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1s. External pullup resistors are required during program verification.
V_{SS}	22	16	–	**Circuit ground potential**
V_{CC}	44	38	–	**Power Supply terminal** for all operating modes
N.C.	1, 12, 23, 34	6, 17, 28, 39	–	**No connection**, do not connect externally

*) I = Input
O = Output

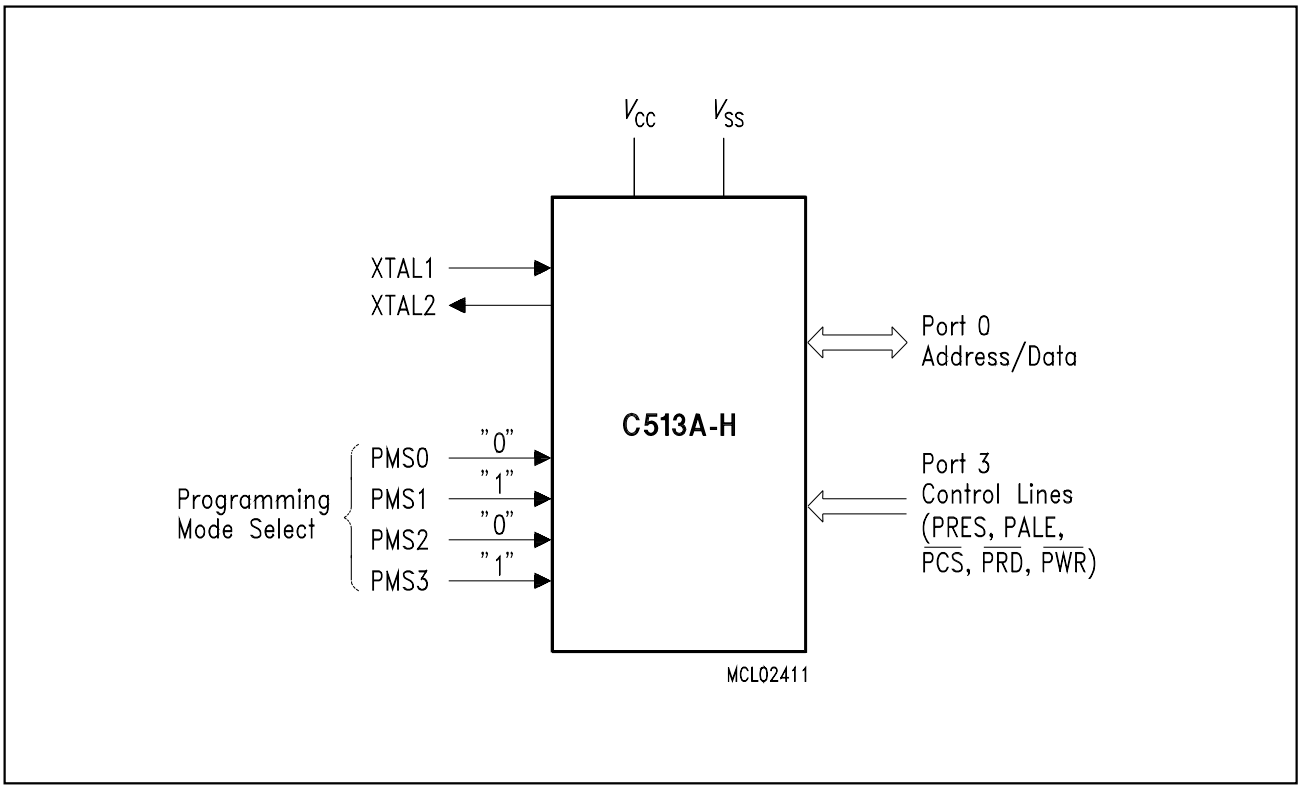


Figure 4
C513A-H Logic Symbol in Programming Mode

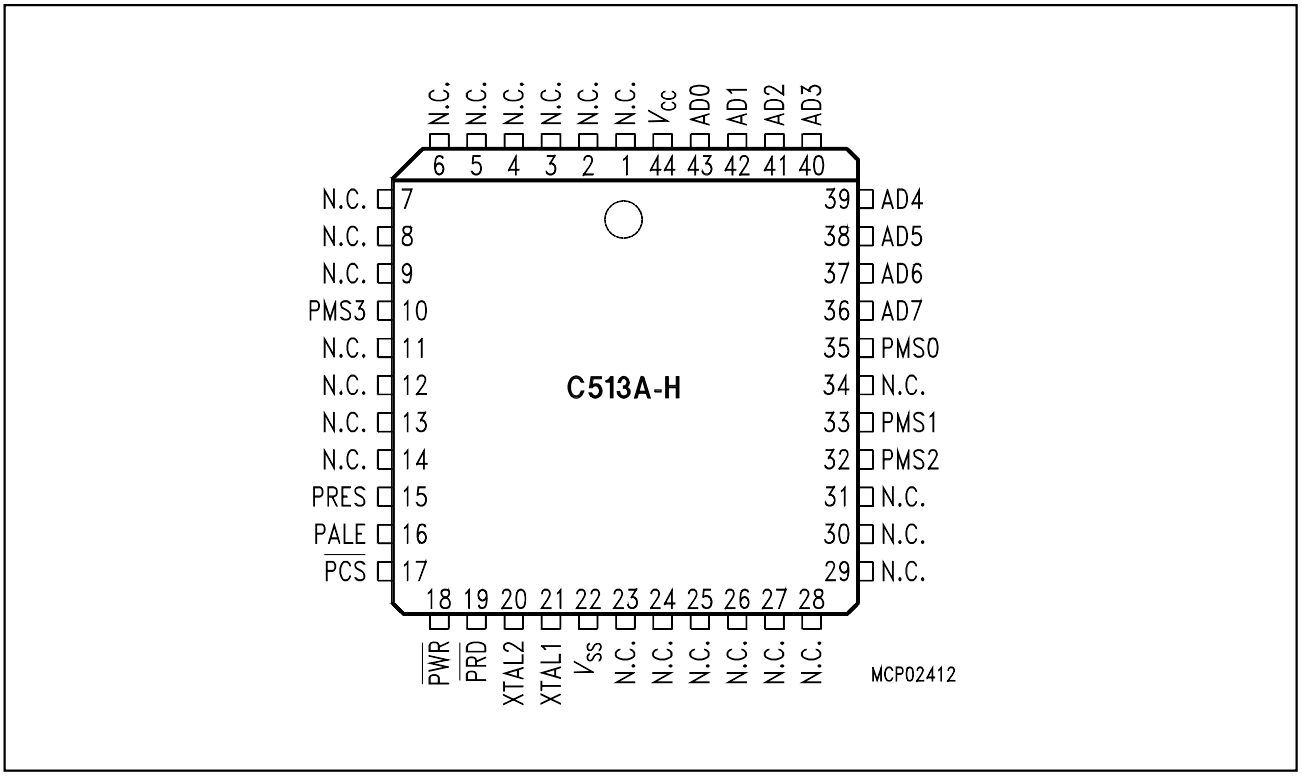


Figure 5
C513A-H Pin Configuration in Programming Mode (P-LCC-44)

Table 4
Pin Definitions and Functions in Programming Mode (C513A-H only)

Symbol	Pin Number P-LCC-44	I/O*)	Function
PRES	15	I	**Programming Interface Reset** A high level on this input resets the programming interface and its registers to their initial state.
AD0 - AD7	43 - 36	I/O	**Bidirectional Address/Data Bus** AD0-7 is used to transfer data to and from the registers of the programming interface and to read the data of the memory field during EEPROM verification.
PALE	16	I	**Programming Address Latch Enable** This input is used to latch address information at AD0-7. The trailing edge of PALE is used to latch the register addresses. Each read or write access in programming mode must be initiated by a PALE high pulse.
$\overline{\text{PRD}}$	18	I	**$\overline{\text{Programming Read Control}}$** A low level at this pin (and $\overline{\text{PCS}}$=low) enables the AD0-7 buffers for reading of the data or control registers of the programming interface.
$\overline{\text{PWR}}$	19	I	**$\overline{\text{Programming Write Control}}$** A low level at this pin (and $\overline{\text{PCS}}$=low) causes the data at AD0-7 to be written into the data or control registers of the programming interface.
$\overline{\text{PCS}}$	17	I	**$\overline{\text{Programming Chip Select}}$** A low level at this pin enables the access to the registers of the programming interface. If $\overline{\text{PCS}}$ is active, either $\overline{\text{PRD}}$ or $\overline{\text{PWR}}$ control whether data is read or written into the registers. $\overline{\text{PCS}}$ should be always deactivated between subsequent accesses to the programming interface.
XTAL2	20	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	21	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. During the device programming a clock must be always supplied.

*) I = Input
O = Output

Table 4
Pin Definitions and Functions in Programming Mode (C513A-H only) (cont'd)

<table>
<tr><th>Symbol</th><th>Pin Number
P-LCC-44</th><th>I/O*)</th><th>Function</th></tr>
<tr><td>PMS0
PMS1
PMS2
PMS3</td><td>35
33
32
10</td><td>I</td><td>Programming Mode Select
PMS0-3 are used to put the C513A-H into the program-ming mode. In normal mode the programming mode select pins have the meaning as shown in the table below. PMS0-3 must be set to the logic level as described in the table below.

<table><tr><th>Normal Mode Pin Names</th><th>Progr. Mode Pin Names</th><th>Required Logic Level</th></tr><tr><td>$\overline{EA}$</td><td>PMS0</td><td>0</td></tr><tr><td>ALE</td><td>PMS1</td><td>1</td></tr><tr><td>$\overline{PSEN}$</td><td>PMS2</td><td>0</td></tr><tr><td>RESET</td><td>PMS3</td><td>1</td></tr></table></td></tr>
<tr><td>V_{SS}</td><td>22</td><td>–</td><td>Circuit ground potential</td></tr>
<tr><td>V_{CC}</td><td>44</td><td>–</td><td>Power supply terminal for all operating modes</td></tr>
<tr><td>N.C.</td><td>1-9, 11-14, 23-31, 34</td><td>–</td><td>No connection
These pins must not be connected.</td></tr>
</table>

*) I = Input
O = Output

Functional Description

The C511/C513 microcontrollers are fully compatible to the standard 8051/80C52 and C500 microcontroller family. While maintaining all architectural and operational characteristics of the 80C52/C500 the C511/C513 incorporates enhancements such as additional internal XRAM and a second (synchronous) serial interface unit.

Figure 6 shows a block diagram of the C511/C513 microcontroller family.

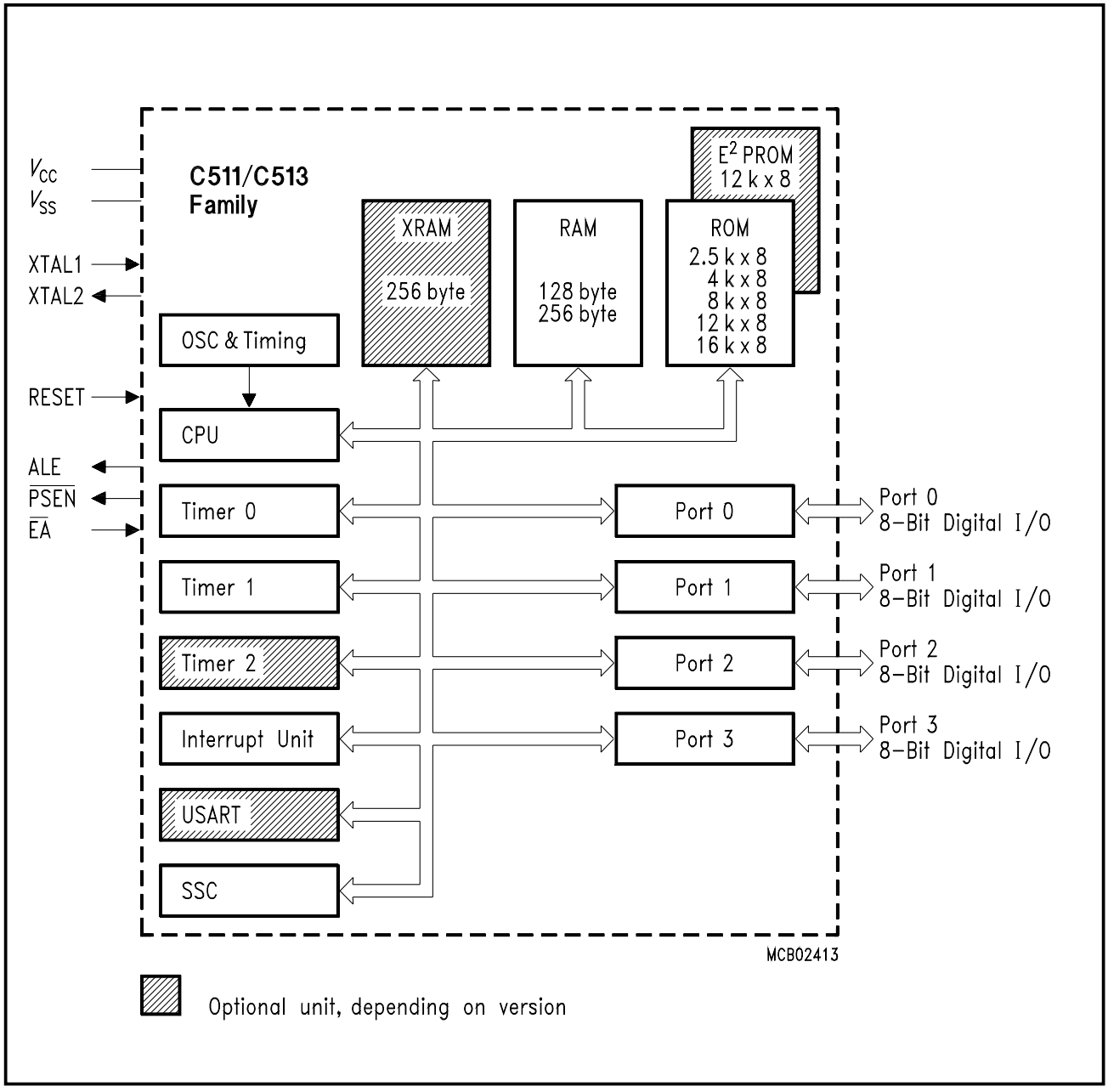


Figure 6
Block Diagram of the C511/C513 Units

CPU

The C511/C513 are efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and for bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions execute in 1 µs.

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		Carry Flag
AC		Auxiliary Carry Flag (for BCD operations)
F0		General Purpose Flag
RS1	RS0	Register Bank select control bits
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$
OV		Overflow Flag
F1		General Purpose Flag
P		Parity Flag Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Special Function Registers

All registers except the program counter and the four general purpose register banks reside in the special function register area.

The 34 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 5** and **table 6**. In **table 5** they are organized in groups which refer to the functional blocks of the C511/C513. **Table 6** illustrates the contents of the SFRs, e.g. the bits of the SFRs, in numeric order of their addresses.

Table 5
SFRs - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	**00_H**
	B	B-Register	**$F0_H$** [1]	**00_H**
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word	**$D0_H$** [1]	**00_H**
	SP	Stack Pointer	81_H	07_H
	SYSCON	System Control Reg. C511/C511A/C513	$B1_H$	$101X0XXX_B$ [3]
		C513A/C513A-H	$B1_H$	$101X0XX0_B$ [3]
Interrupt System	IE	Interrupt Enable Register	**$A8_H$** [1]	**00_H**
	IP	Interrupt Priority Register	**$B8_H$** [1]	**$X0000000_B$** [3]
Ports	P0	Port 0	**80_H** [1]	**FF_H**
	P1	Port 1	**90_H** [1]	**FF_H**
	P2	Port 2	**$A0_H$** [1]	**FF_H**
	P3	Port 3	**$B0_H$** [1]	**FF_H**
SSC	SSCCON	SSC Control Register	**$E8_H$** [1]	**07_H**
	STB	SSC Transmit Buffer	$E9_H$	XX_H [3])
	SRB	SSC Receive Register	EA_H	XX_H [3])
	SCF	SSC Flag Register	**$F8_H$** [1]	**$XXXXXX00_B$** [3]
	SCIEN	SSC Interrupt Enable Register	$F9_H$	$XXXXXX00_B$ [3]
	SSCMOD	SSC Mode Test Register	EB_H	00_H
USART	PCON [2]	Power Control Register	87_H	$0XXX0000_B$ [3]
	SBUF	Serial Channel Buffer Register	99_H	XX_H [3])
	SCON	Serial Channel 1 Control Register	**98_H** [1]	00_H
Timer 0 / Timer 1	TCON	Timer Control Register	**88_H** [1]	**00_H**
	TMOD	Timer Mode Register	89_H	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
	T2MOD	Timer 2 Mode Register	$C9_H$	$XXXXXXX0_B$ [3]
	RC2L	Timer 2 Reload/Capture Register, Low Byte	CA_H	00_H
	RC2H	Timer 2 Reload/Capture Register, High Byte	CB_H	00_H
	TL2	Timer 2 Low Byte	CC_H	00_H
	TH2	Timer 2 High Byte	CD_H	00_H
Power Save Mode	PCON [2]	Power Control Register	87_H	$0XXX0000_B$ [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 6
Contents of the SFRs, SFRs in Numeric Order of their Addresses

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	$0XXX\text{-}0000_B$	SMOD	–	–	–	GF1	GF0	PDE	IDLE
88_H	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H	P1	FF_H	–	–	$\overline{SLS}$	STO	SRI	SCLK	T2EX	T2
98_H	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$	IE	00_H	EAL	ESSC	ET2	ES0	ET1	EX1	ET0	EX0
$B0_H$	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
$B1_H$	SYSCON	[2]	1	0	EALE	–	0	–	–	XMAP[2]
$B8_H$	IP	$X000\text{-}0000_B$	–	PSSC	PT2	PS	PT1	PX1	PT0	PX0
$C8_H$	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	$XXXX\text{-}XXX0_B$	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$E0_H$	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$	SSCCON	07_H	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
$E9_H$	STB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EA_H	SRB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EB_H	SSCMOD	00_H [3]	0	0	0	0	0	0	0	0
$F0_H$	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0

Table 6
Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr	Register	Content after Reset [1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F8_H$	SCF	XXXX-XX00_B	–	–	–	–	–	–	WCOL	TC
$F9_H$	SCIEN	XXXX-XX00_B	–	–	–	–	–	–	WCEN	TCEN

1) X means that the value is indeterminate and the location is reserved.
2) The availability of the XMAP bit and the reset value of SYSCON depends on the specific microcontroller :
C511/C511A/C513 : $101X0XXX_B$ - bit XMAP is not available
C513A/C513A-H : $101X0XX0_B$ - bit XMAP is available
3) This register ist only used for test purposes and must not be written. Otherwise unpredictable results may occur.
Shaded registers are bit-addressable special function registers.

Timer/ Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 7**:

Table 7
Timer/Counter 0 and 1 operating modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/_{12 \times 32}$	$f_{OSC}/_{24 \times 32}$
1	16-bit timer/counter	X	X	0	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
2	8-bit timer/counter with 8-bit auto-reload	X	X	1	0	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$

In “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 7** illustrates the input clock logic.

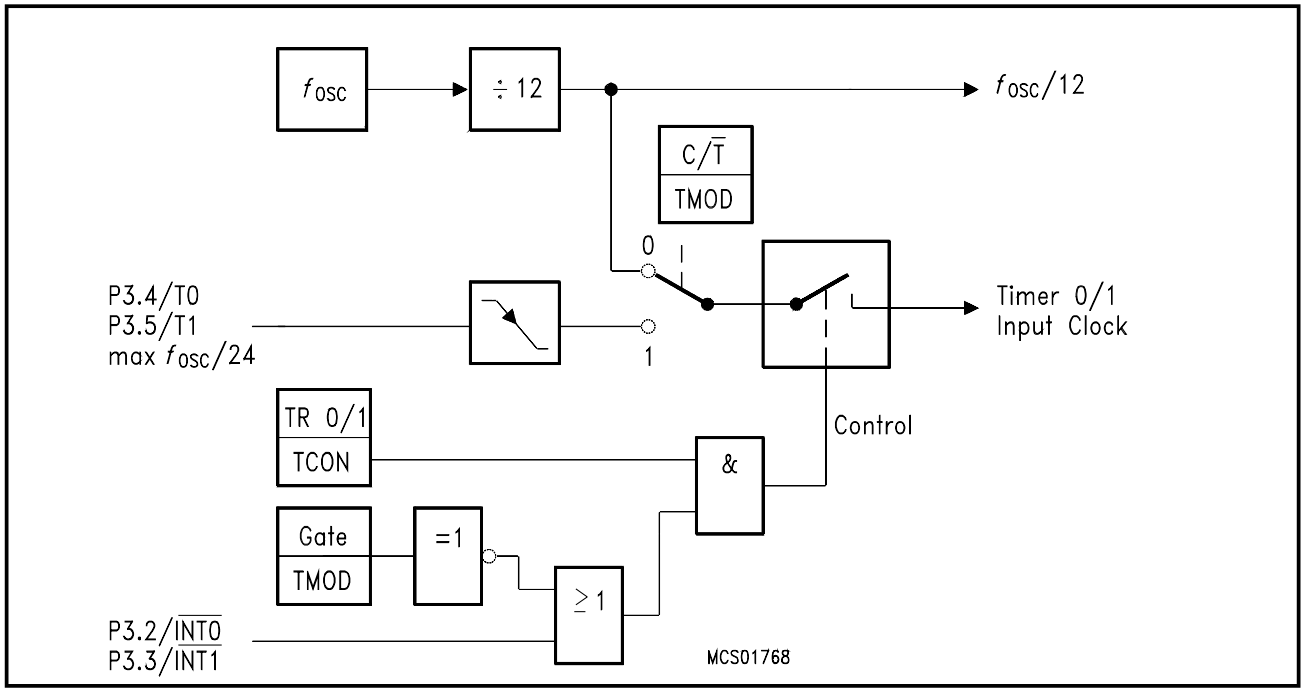


Figure 7
Timer/Counter 0 and 1 Input Clock Logic

Timer / Counter 2 (not available in the C511/C511A)

Timer 2 is a 16-bit Timer/Counter with up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in **table 8**.

Table 8
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/$\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{osc}/12	max f_{osc}/24
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Cap-ture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting) capture TH2, TL2 → RC2H, RC2L	f_{osc}/12	max f_{osc}/24
	0	1	1	X	1	↓			
Baud Rate Gene-rator	1	X	1	X	0	X	no overflow interrupt request (TF2) extra external interrupt (“Timer 2”)	f_{osc}/2	max f_{osc}/24
	1	X	1	X	1	↓			
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Serial Interface (USART, not available in the C511/C511A)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 9**. **Figure 8** illustrates the block diagram of Baudrate generation for the serial interface.

Table 9
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

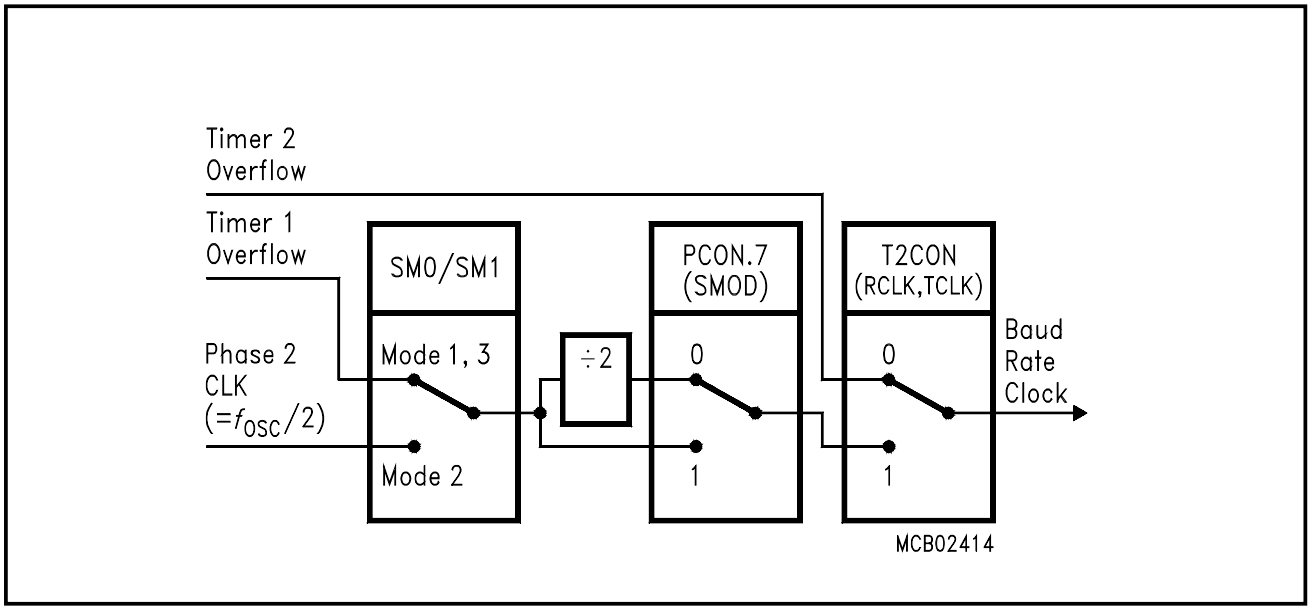


Figure 8
Block Diagram of Baud Rate Generation for the Serial Interface

The possible baudrates can be calculated using the formulas given in **table 10**.

Table 10
Baudrates Selection

Baud rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC})/64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate$)/32$ $(2^{SMOD} \times f_{OSC})/(32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	$f_{OSC}/(32 \times (65536\text{-(RC2H, RC2L)}))$

Synchronous Serial Channel (SSC)

The C511/C513 microcontrollers provide a Synchronous Serial Channel unit, the SSC. This interface is compatible to the popular SPI serial bus interface. It can be used for simple I/O expansion via shift registers, for connection of a variety of peripheral components, such as A/D converters, EEPROMs etc., or for allowing several microcontrollers to be interconnected in a master/slave structure. It supports full-duplex or half-duplex operation and can run in a master or a slave mode. **Figure 9** shows the block diagram of the SSC.

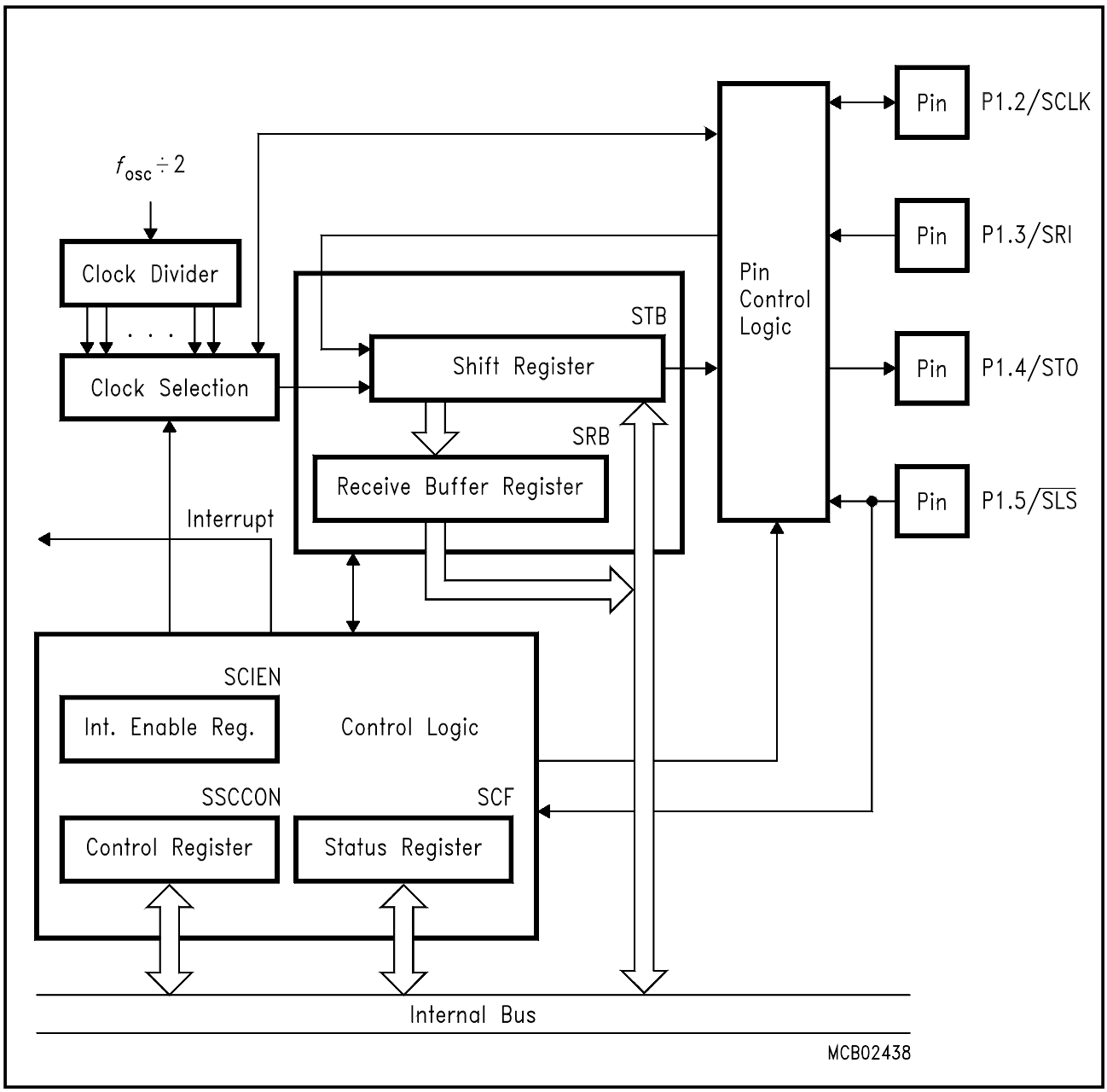


Figure 9
SSC Blockdiagram

Additional On-Chip XRAM (not available in the C511/C511A/C513)

The C513A/C513A-H contain another 256 byte of on-chip RAM additional to the 256 byte internal RAM. This RAM is called XRAM ('e**X**tended **RAM**').

The additional on-chip XRAM is logically located in the external data memory range from address $FF00_H$ to $FFFF_H$. The contents of the XRAM are not affected by a reset. After power up the content is undefined, while it remains unchanged during and after reset as long as the power supply is not turned off. The XRAM is controlled by SFR SYSCON as shown in **table 11**.

Table 11
Control of the XRAM

SFR SYSCON Bit XMAP	Description
0	Reset value. Access to XRAM is disabled.
1	XRAM enabled. The signals $\overline{RD}$ and $\overline{WR}$ are not activated during MOVX accesses in the XRAM address range.

The XRAM is accessed as external data memory. Therefore, MOVX instruction types must be used for accessing the XRAM. A general overview gives **table 12**.

Table 12
Accessing the XRAM

Instruction using	Instruction	Remarks
DPTR (16-bit addr.)	MOVX A @DPTR MOVX @DPTR,A	Normally the use of these instructions would use a physically external memory. However, in the C513A/ C513A-H the XRAM is accessed if it is enabled by bit XMAP and the 16-bit address (DPTR) is within the XRAM address range $FF00_H$ - $FFFF_H$.
R0/R1 (8-bit addr.)	MOVX A, @Ri MOVX @Ri,A	If XRAM is enabled in the C513A/C513A-H, MOVX instructions using Ri will always access the internal XRAM. External data memory cycles will not be generated in this case. If the XRAM is disabled, MOVX instructions using Ri will generate normal external data memory cycles.

Interrupt System

The C511/C513 provide 7 interrupt sources with two priority levels. **Figure 10** gives a general overview of the interrupt sources and illustrates the request and control flags.

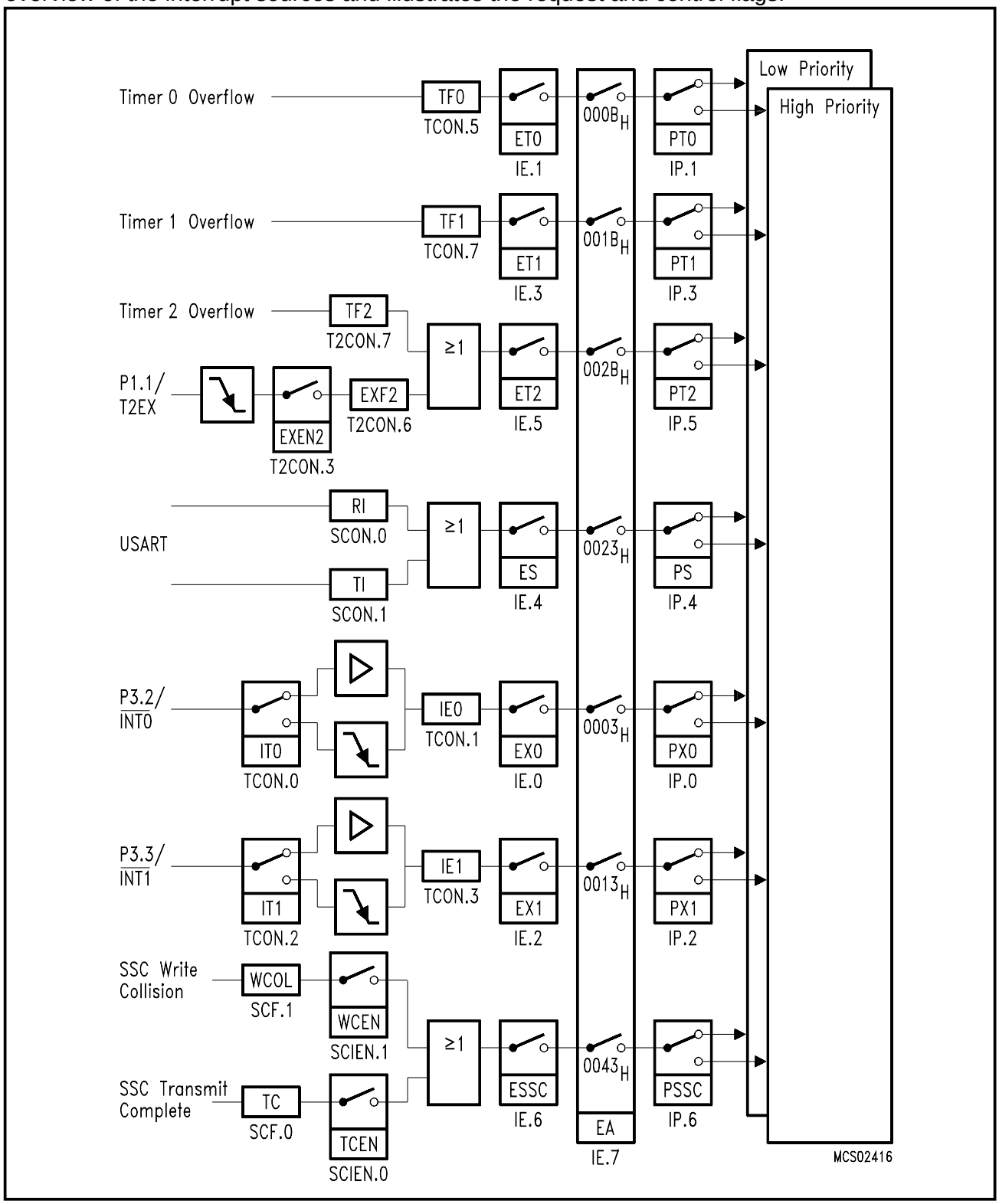


Figure 10
Interrupt Request Sources

Table 13
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	USART serial port interrupt, (C513/C513A/C513A-H only)	0023_H
TF2 + EXF2	Timer 2 interrupt	
SSCI	Synchronous serial channel interrupt (SSC)	$002B_H$ 0043_H

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 14**.

Table 14
Priority-within-Level Structure

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Synchronous Serial Channel	SSC	
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Universal Serial Channel,	RI or TI	
Timer 2 Interrupt,	TF2 or EXF2	Low

Power Saving Modes

Two power down modes are available, the idle mode and the power down mode. In the idle mode only the CPU will be deactivated while in the power down mode the on-chip oscillator is stopped.

The bits PDE and IDLE select the power down mode or the idle mode, respectively. If the power down mode and the idle mode are set at the same time, power down takes precedence. **Table 15** gives a general overview of the power saving modes.

Table 15
Entering and leaving the power saving modes

Mode	Entering Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power Down Mode	ORL PCON, #02H	Hardware Reset	Oscillators are stopped. Contents of on-chip RAM and SFR's are maintained (leaving power down mode means redefinition of SFR's contents)

In the power down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power down mode is terminated. The reset signal that terminates the power down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 ˚C to + 70 ˚C
Storage temperature (T_{ST}) .....– 65 ˚C to + 150 ˚C

Voltage on V_{CC} pins with respect to ground (V_{SS}) .....– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....– 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition.....– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....| 100 mA |

Power dissipation.....TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 to + 70 ˚C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{EA}$, RESET, XTAL1)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage Ports 1, 2, 3 (except P1.2, P1.4) Port 0, ALE, $\overline{PSEN}$ P1.2 / P1.4 pull-down transistor resistance	 V_{OL} V_{OL1} R_{DSon}	 – – –	 0.45 0.45 120	 V V Ω	 I_{OL} = 1.6 mA [1] I_{OL} = 3.2 mA [1] V_{OL} = 0.45 V
Output high voltage Ports 1, 2, 3 Port 0 in ext. bus mode, ALE, $\overline{PSEN}$ P1.2 / P1.4 pull-up transistor resistance	 V_{OH} V_{OH1} R_{DSon}	 2.4 0.9 V_{CC} 2.4 0.9 V_{CC} –	 – – – – 120	 V V V V Ω	 I_{OH} = – 80 µA I_{OH} = – 10 µA I_{OH} = – 800 µA I_{OH} = – 80 µA V_{OH} = 0.9 V_{CC}
Logic 0 input current (Ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (Ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Maximum output low current per pin (Ports 0, 1, 2, 3)	I_{OLM}	–	5	mA	$V_{OL} \leq$ 1 V
Maximum output low current per port	I_{PL}	–	30	mA	–
Input leakage current Port 0 (if $\overline{EA}$=0), $\overline{EA}$, P1.2, P1.3, P1.5 as SSC inputs	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance [7]	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 ˚C

DC Characteristics (cont'd)

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 to + 70 ˚C

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. [8]	max.		
Power supply current:					
C511/C511A/C513/C513A					
Active mode, 12 MHz [6]	I_{CC}	7	9.5	mA	V_{CC} = 5 V,[4]
Idle mode, 12 MHz [6]	I_{CC}	3.5	4.5	mA	V_{CC} = 5 V,[5]
Power Down Mode	I_{PD}	TBD	50	µA	V_{CC} = 2 … 5.5 V,[3]
C513A-H					
Active mode, 12 MHz [6]	I_{CC}	16	TBD	mA	V_{CC} = 5 V,[4]
Idle mode, 12 MHz [6]	I_{CC}	6	TBD	mA	V_{CC} = 5 V,[5]
Power Down Mode	I_{PD}	TBD	50	µA	V_{CC} = 2 … 5.5 V[3]

Notes:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{CC}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

6) $I_{CC\,Max}$ at other frequencies is given by:

C511/C511A/C513/C513A :	Active mode:	TBD
	Idle mode:	TBD
C513A-H :	Active mode:	TBD
	Idle mode:	TBD

where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

7) This parameter is periodically sampled and not 100% tested.

8) The typical I_{CC} values are periodically measured at T_A = +25 ˚C but not 100% tested.

AC Characteristics (applies to all C511/513 Family Microcontrollers)

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 ˚C to + 70 ˚C

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}$ – 40	–	ns
Address setup to ALE	t_{AVLL}	43	–	t_{CLCL} – 40	–	ns
Address hold after ALE	t_{LLAX}	60	–	t_{CLCL} – 23	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL}$ – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL}$ – 35	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL}$ – 100	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	t_{CLCL} – 8	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL}$ – 115	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C511/513 microcontrollers to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

SSC Interface Characteristics

Parameter	Symbol	Limit Values		Unit
		12 MHz Clock		
		min.	max.	
Clock Cycle Time : Master Mode Slave Mode	t_{SCLK} t_{SCLK}	666 600	– –	ns ns
Clock high time	t_{SCH}	250	–	ns
Clock low time	t_{SCL}	250	–	ns
Data output delay	t_{D}	–	100	ns
Data output hold	t_{HO}	0	–	ns
Data input setup	t_{S}	100	–	ns
Data input hold	t_{HI}	100	–	ns
TC bit set delay	t_{DTC}	–	16 t_{CLCL}	ns

External Clock Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

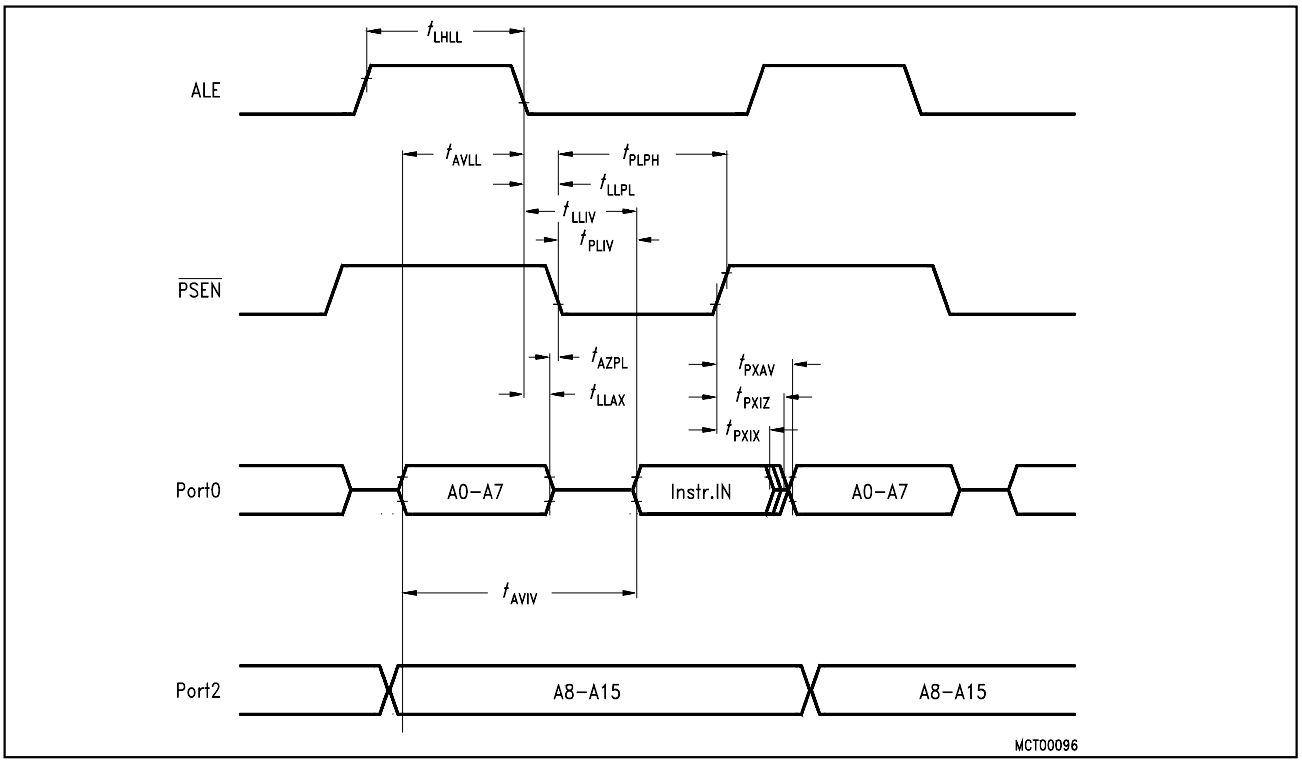


Figure 11
Program Memory Read Cycle

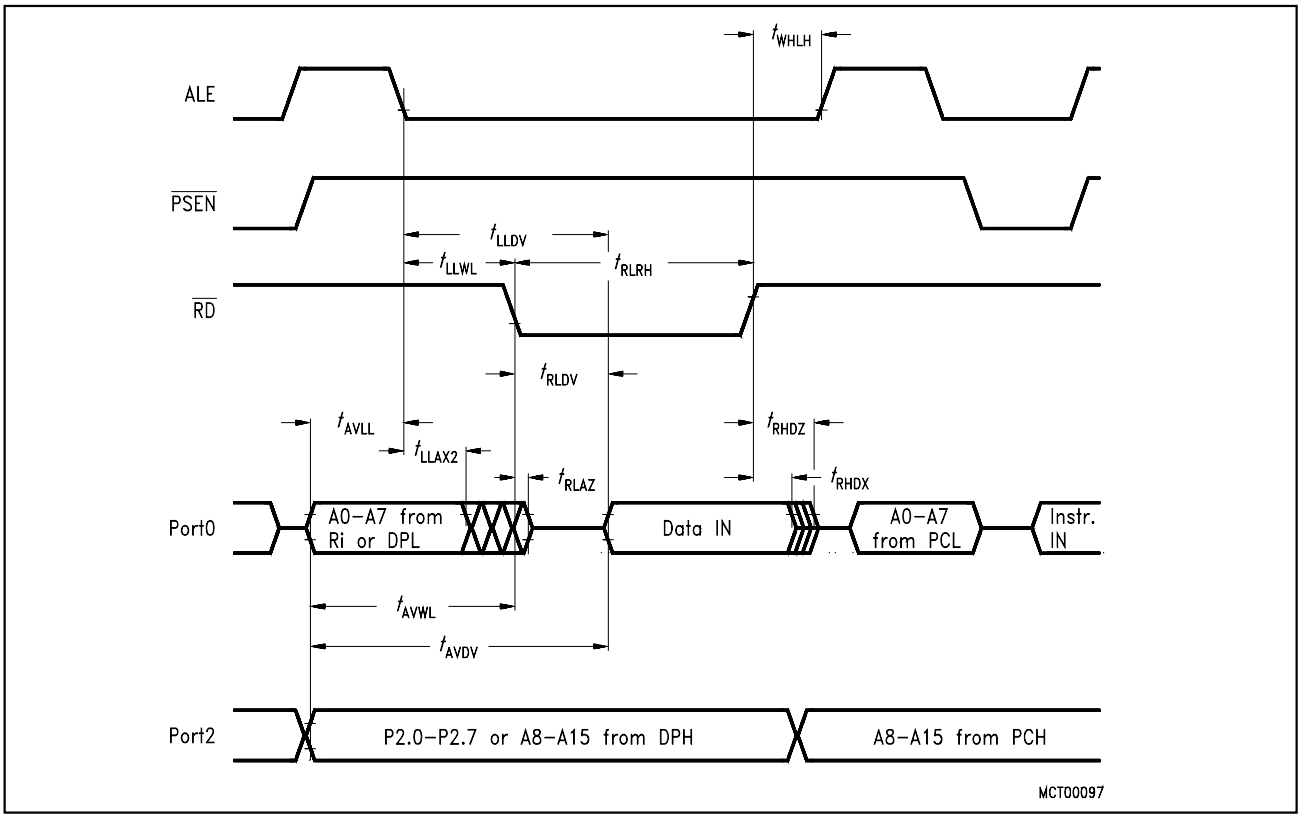


Figure 12
Data Memory Read Cycle

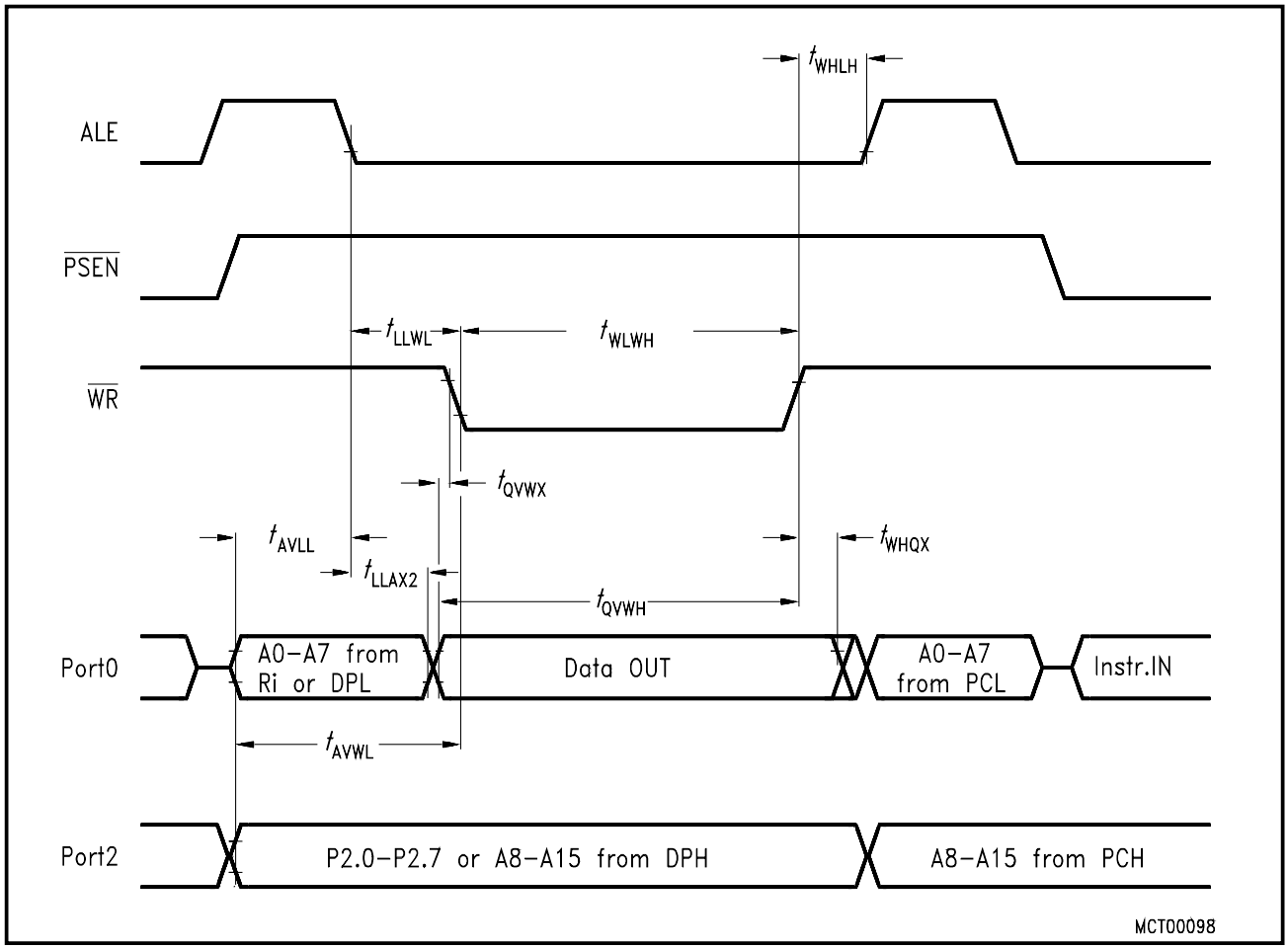
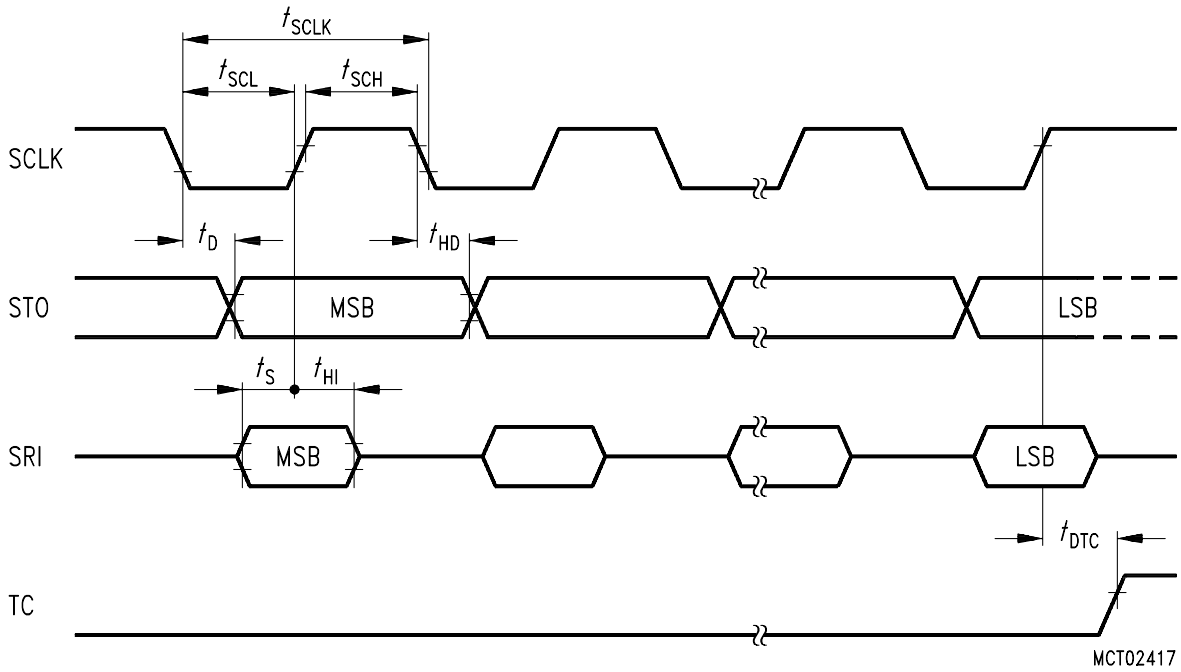


Figure 13
Data Memory Write Cycle



Notes: Shown is the data/clock relationship for CPOL = CPHA = 1. The timing diagram is valid for the other cases accordingly.

In the case of slave mode and CPHA = 0, the output delay for the MSB applies to the falling edge of $\overline{SLS}$ (if transmitter is enabled).

In the case of master mode and CPHA = 0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.

Figure 14
SSC Timing

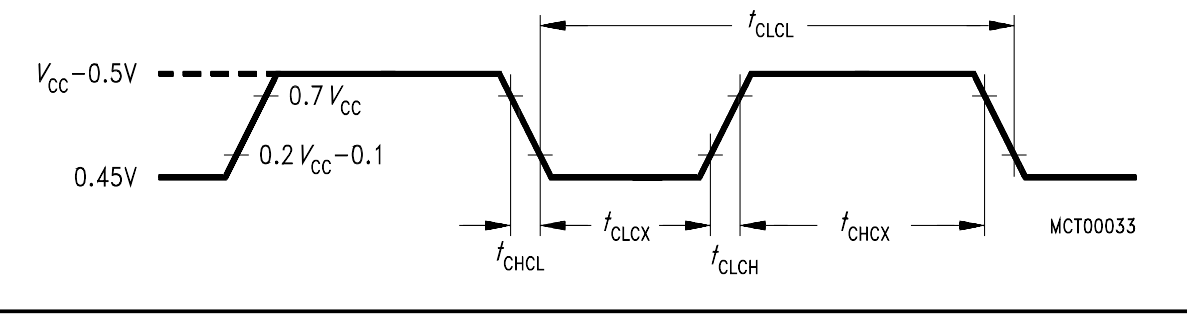
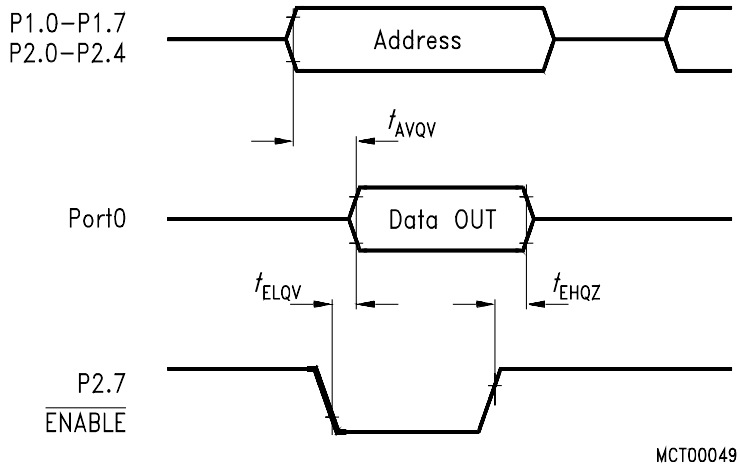


Figure 15
External Clock Drive at XTAL1

ROM Verification Characteristics (only ROM versions C511 / C511A / C513 / C513A)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

Inputs: P2.5–P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA}=V_{IH}$
RESET = V_{IH1}

Device Type	ROM Size	Active Address Lines at Port 2	Inactive Address Lines at Port 2
C511	2.5 KB	P2.0 - P2.3 = A8 - A11	P2.4 - P2.6 = V_{SS}
C511A	4 KB	P2.0 - P2.3 = A8 - A11	P2.4 - P2.6 = V_{SS}
C513	8 KB	P2.0 - P2.4 = A8 - A12	P2.5 - P2.6 = V_{SS}
C513A	12/16 KB	P2.0 - P2.5 = A8 - A13	P2.6 = V_{SS}

Figure 16
ROM Verification Timing

AC Characteristics of C513A-H Programming Interface

V_{CC} = 5 V ± 10 %, V_{SS} = 0 V; T_A = +25 °C ± 10 °C; 1/tCLCL = 8 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{PLL}	60	–	ns
Address setup to ALE	t_{PAL}	20	–	ns
Address hold after ALE	t_{PLA}	20	–	ns
Address to valid data out	t_{PAD}	–	230	ns
$\overline{PRD}$/$\overline{PWR}$ pulse width	t_{PCC}	250	–	ns
$\overline{PRD}$ to valid data out	t_{PRDV}	–	200	ns
Data hold after $\overline{PWR}$	t_{PWDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDZ}	–	40	ns
Chip select setup to ALE active	t_{PCS}	0	–	ns
Chip select hold after $\overline{PRD}$/$\overline{PWR}$ inactive	t_{PCH}	0	–	ns
ALE to $\overline{PWR}$ or $\overline{PRD}$	t_{PLC}	90	–	ns
$\overline{PWR}$ or $\overline{PRD}$ high to ALE high	t_{PCL}	20	–	ns
Data setup before $\overline{PWR}$ rising edge	t_{PWDS}	50	–	ns
Data hold after $\overline{PWR}$ rising edge	t_{PWDH}	0	–	ns
Data float after $\overline{PCS}$	t_{PDF}	–	40	ns

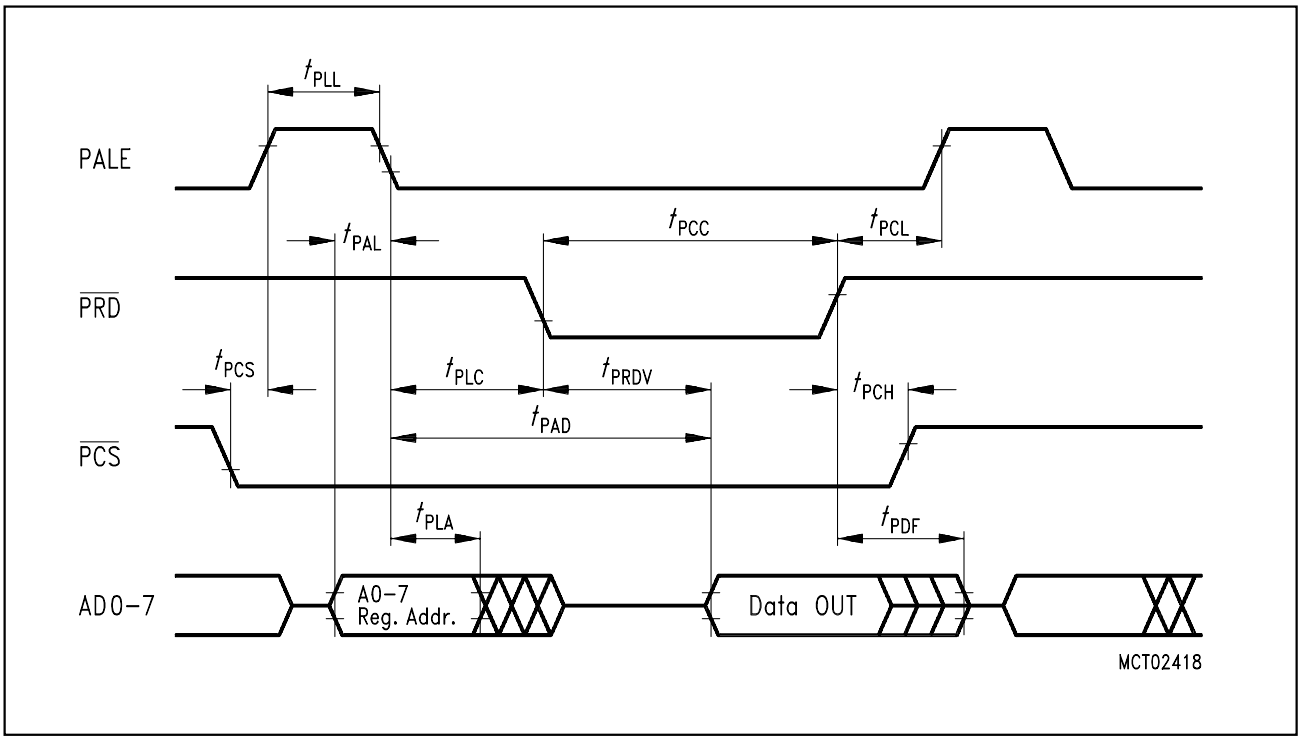


Figure 17
C513A-H Programming Interface Read Cycle

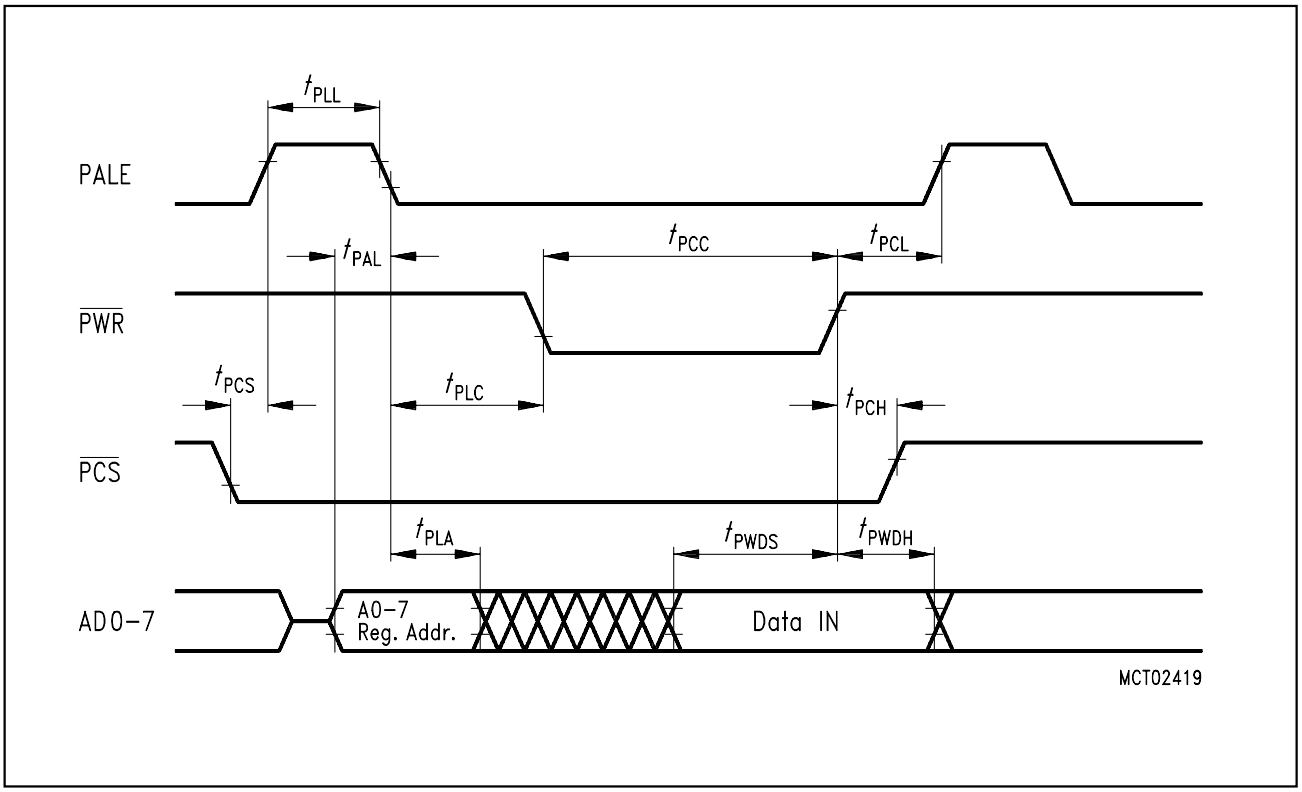


Figure 18
C513A-H Programming Interface Write Cycle

Reset Characteristics (C513A-H only)

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
RESET pulse width	t_{RLRH}	10	–	10	–	ms

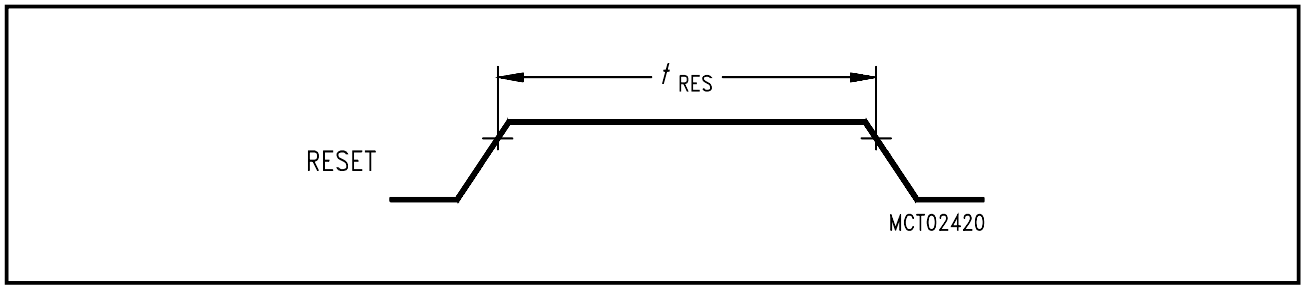
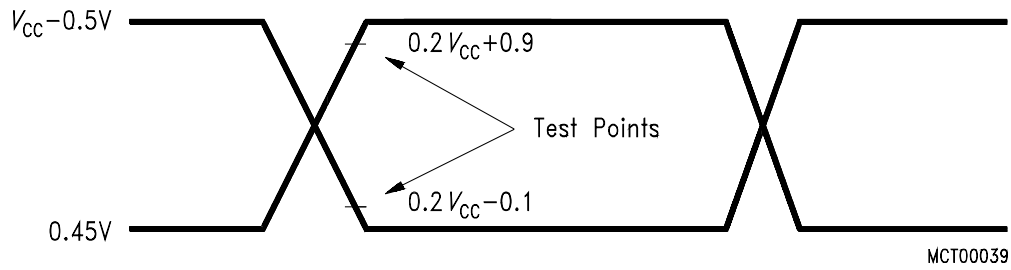
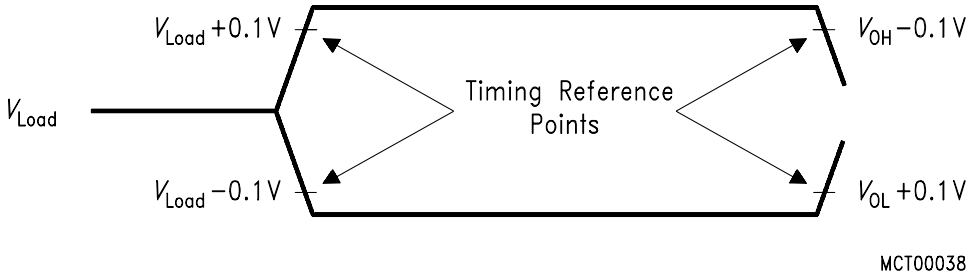


Figure 19
C513A-H Reset Pulse



AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 20
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 21
AC Testing: Float Waveforms

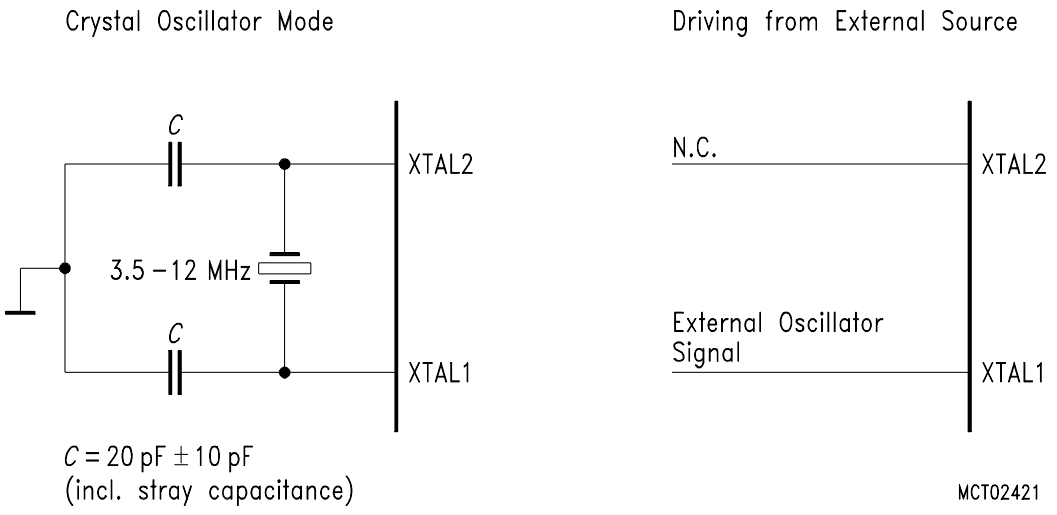


Figure 22
Recommended Oscillator Circuits for Crystal Oscillator