SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C501GV

3 V Specification

Addendum to the C501 Data Sheet 06.97 Advance Information

Edition 06.97

Published by Siemens AG,
Bereich Halbleiter, TS
Balanstraße 73,
81541 München

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 ˚C to + 70 ˚C
Storage temperature (T_{ST}) .....– 65 ˚C to + 150 ˚C

Voltage on V_{CC} pins with respect to ground (V_{SS}) .....– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....– 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition.....– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....| 100 mA |

Power dissipation.....TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 3.3 V + 0.3V, – 0.6V; V_{SS} = 0 V; T_A = 0 to + 70 ˚C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage					
Ports 1, 2, 3	V_{OL1}	–	0.45	V	I_{OL} = 1.6 mA [1]
Port 0, $\overline{EA}$, RESET	V_{OL2}	–	0.45	V	I_{OL} = 3.2 mA [1]
Ports 1, 2, 3	V_{OL3}	–	0.3	V	I_{OL} = 100 µA [1]
Port 0, $\overline{EA}$, RESET	V_{OL4}	–	0.3	V	I_{OL} = 200 µA [1]
Output high voltage					
Ports 1, 2, 3	V_{OH1}	2.0	–	V	I_{OH} = – 20 µA
	V_{OH2}	0.9 V_{CC}	–	V	I_{OH} = – 10 µA
Port 0 in external bus mode, ALE, $\overline{PSEN}$	V_{OH3}	2.0	–	V	I_{OH} = – 800 µA [2]
	V_{OH4}	0.9 V_{CC}	–	V	I_{OH} = – 80 µA [2]
Logic 0 input current (Ports 1, 2, 3)	I_{IL}	– 1	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (Ports 1, 2, 3)	I_{TL}	– 25	– 250	µA	V_{IN} = 2.0 V
Input leakage current Port 0, $\overline{EA}$	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance [6]	C_{IO}	–	10	pF	f_C = 1 MHz T_A = 25 ˚C

Power Supply Current

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.	max.		
Power supply current: [7]					
Active mode, 12 MHz	I_{CC}	6.9	9.4	mA	[4]
Idle mode, 12 MHz	I_{CC}	3.2	4.4	mA	[5]
Power Down Mode	I_{PD}	–	15	µA	V_{CC} = 2 … 3.6 V [3]

Notes :

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading : > 50 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the V_{IL} specification when the address lines are stabilizing.

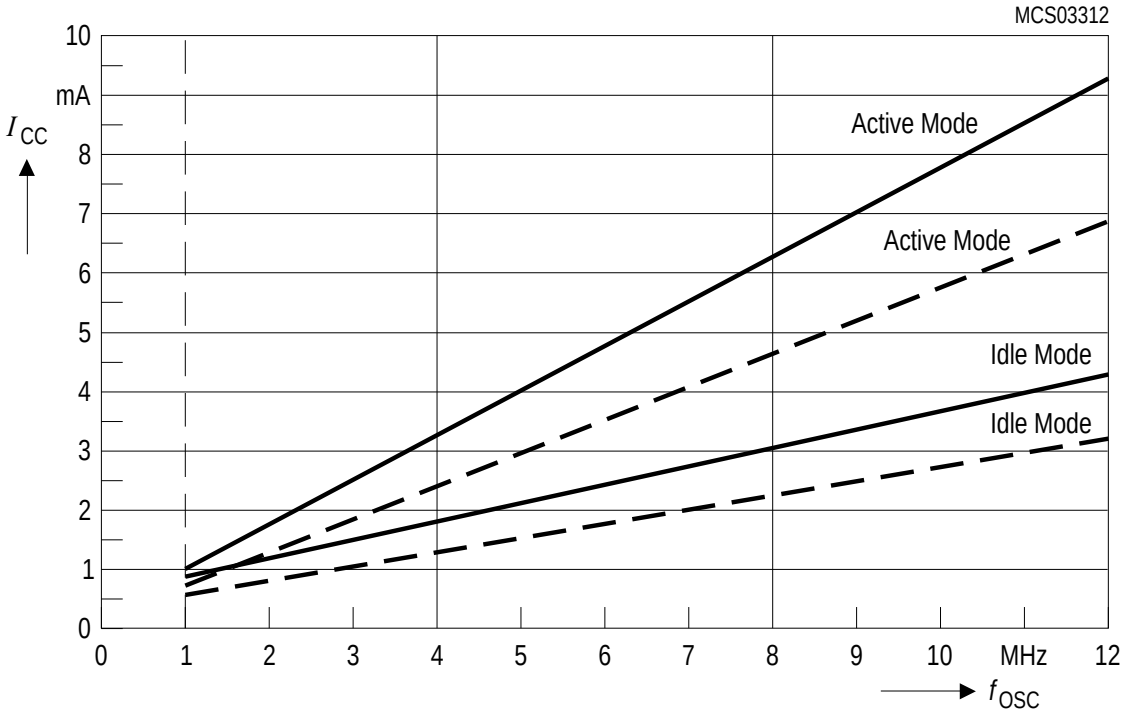
3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 3.3 V.

6) This parameter is periodically sampled and not 100% tested.

7) The typical I_{CC} values are periodically measured at T_A = +25 °C and V_{CC} = 3.0 V but not 100% tested. The maximum I_{CC} values are measured under worst case conditions (V_{CC} = 3.6 V, T_A = 0 °C).



ICC Diagram

AC Characteristics

V_{CC} = 3.3 V + 0.3V, – 0.6V; V_{SS} = 0 V, T_A = 0 °C to + 70 °C
(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 50 pF; C_L for all other outputs = 40 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	30	–	$t_{CLCL} - 53$	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

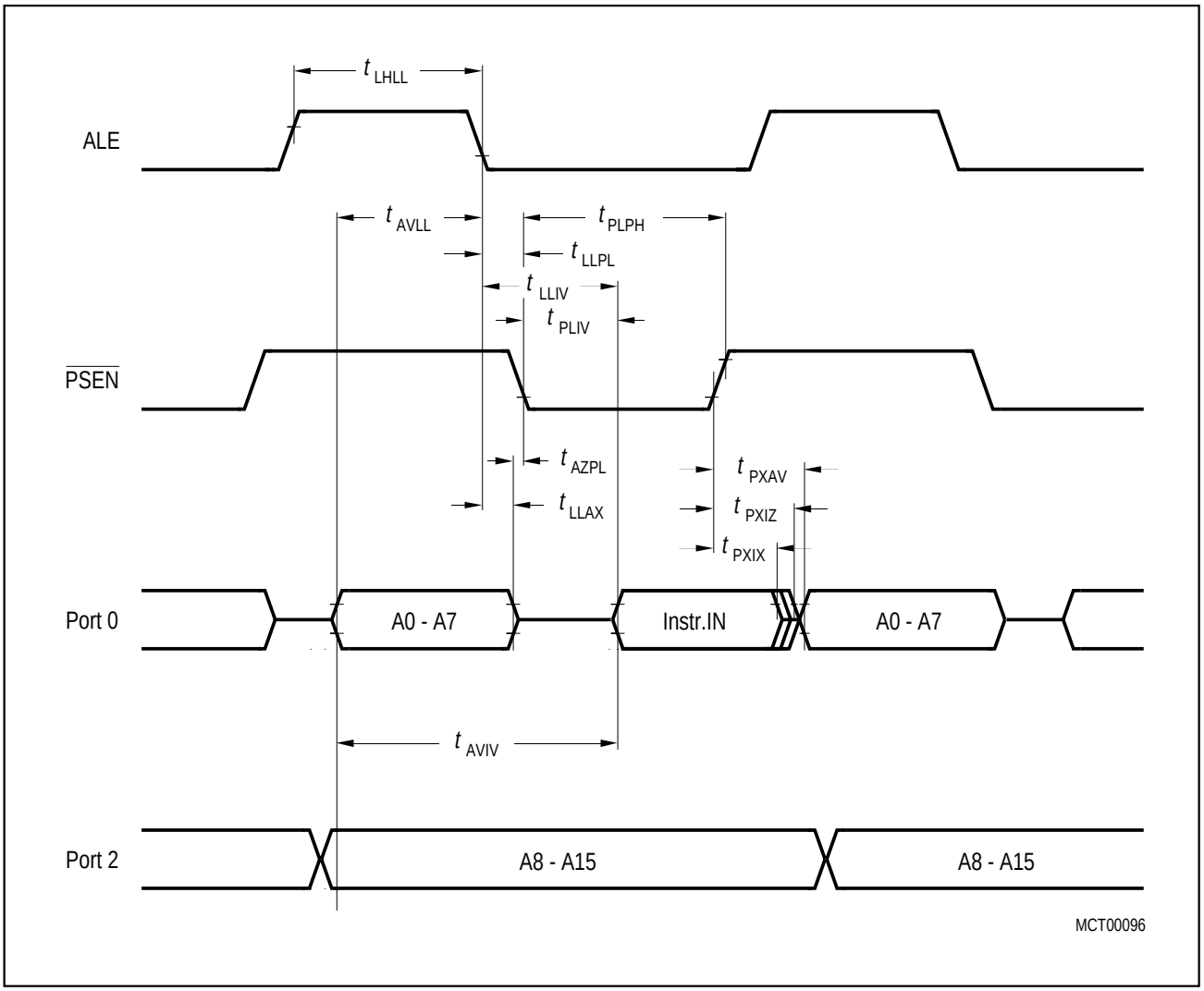
*) Interfacing the C501 microcontrollers to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

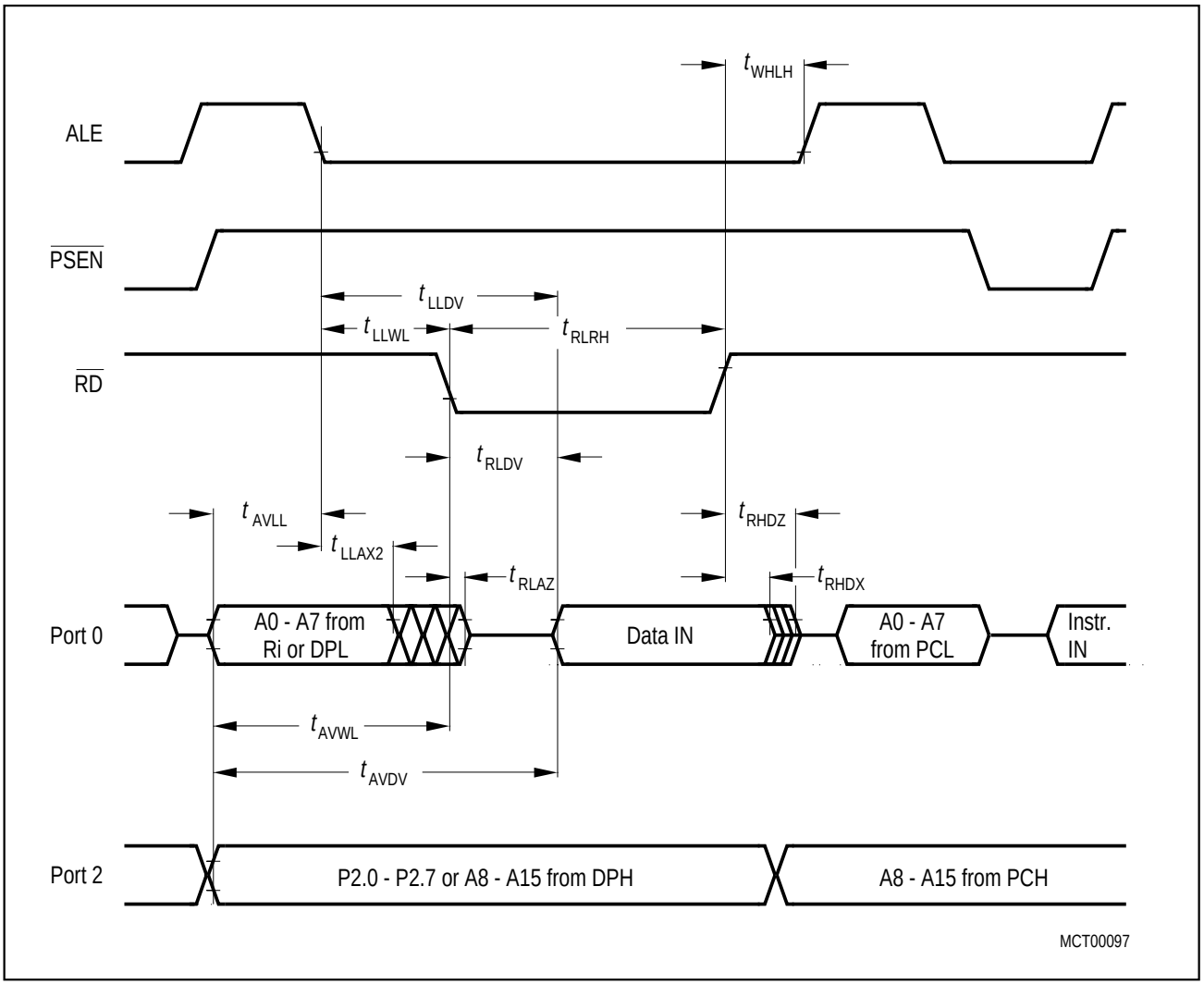
Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	30	–	$t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Characteristics

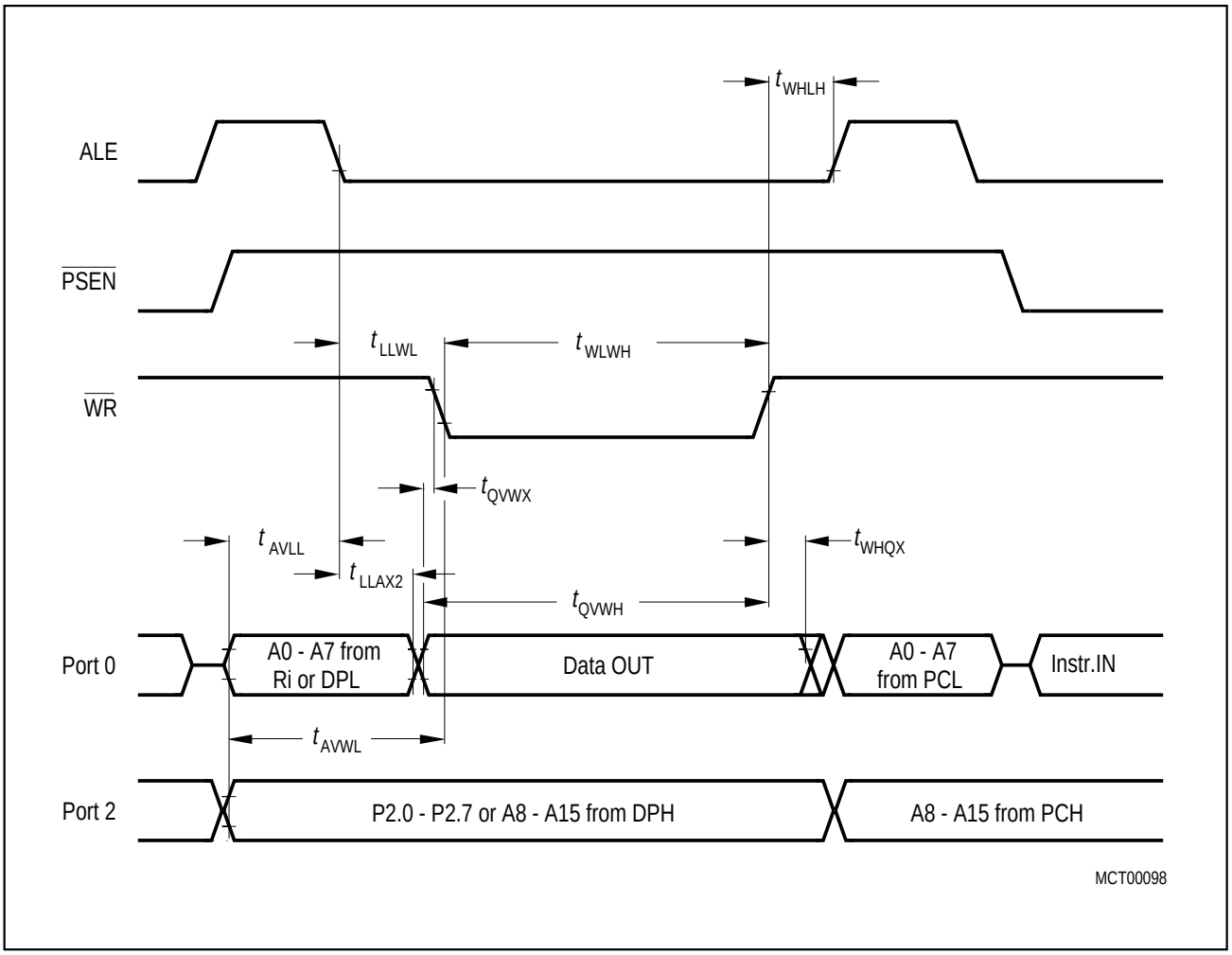
Parameter	Symbol	Limit Values		Unit
		Variable Clock		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	1000	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



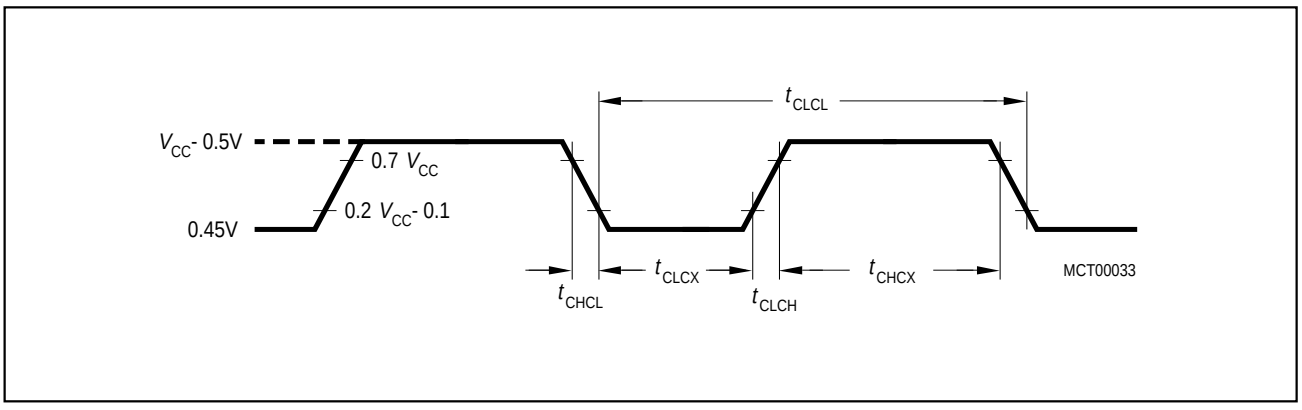
Program Memory Read Cycle



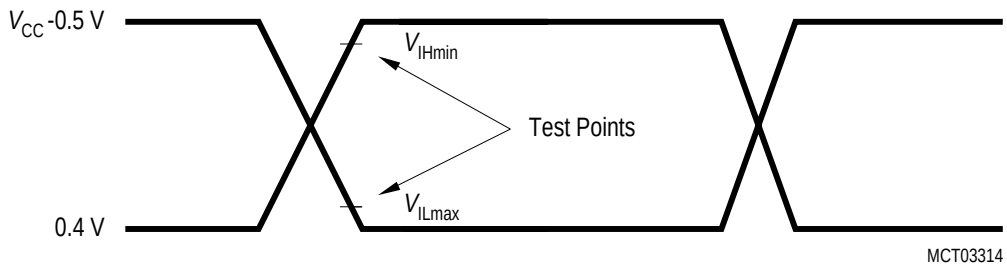
Data Memory Read Cycle



Data Memory Write Cycle

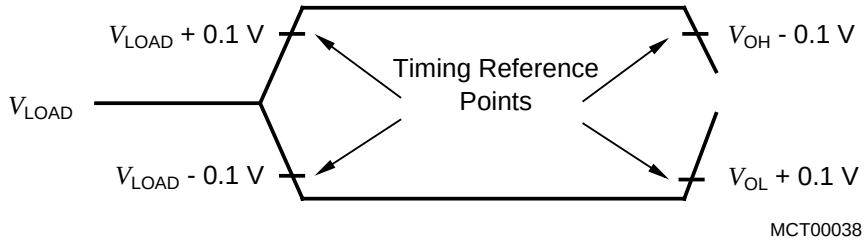


External Clock Drive at XTAL2



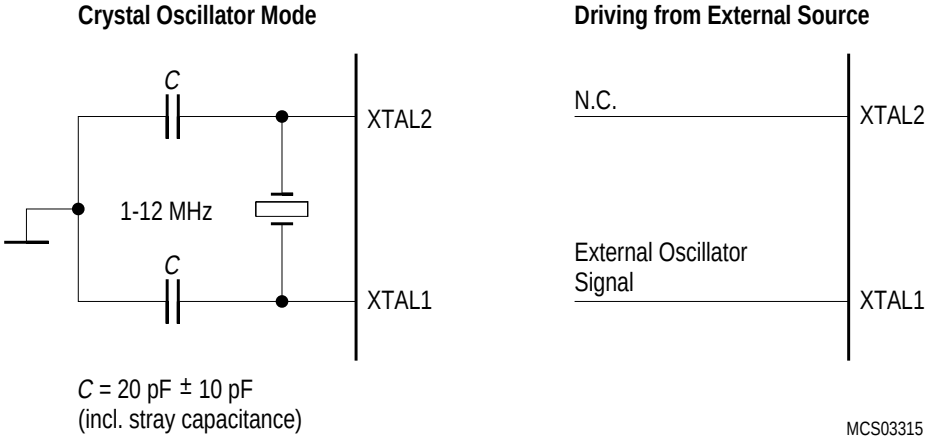
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.4 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

AC Testing: Float Waveforms



Recommended Oscillator Circuits for Crystal Oscillator

Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C501GV-LN SAB-C501GV-LP	Q67120-C2017 Q67120-C2016	P-LCC-44 P-DIP-40	for external memory (12 MHz)