SIEMENS

Microcomputer Components

16-Bit CMOS Single-Chip Microcontroller

Bare Die, Step BA
C167CR/C167SR-LC

Data Sheet 05.97 (Bare Die Delivery)

C167CR-LC/C167SR-LC (Bare Die Delivery) Revision History: Original Version 05.97	
Previous Releases:	-
Page	**Subjects**

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SIEMENS

C16x-Family of
High-Performance CMOS 16-Bit Microcontrollers

C167xR-LC

Advance Information
C167xR-LC 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- 500 ns Multiplication (16 × 16 bit), 1 µs Division (32 / 16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via on-chip PLL or via direct clock input
- Up to 16 MBytes Linear Address Space for Code and Data
- 2 KBytes On-Chip Internal RAM (IRAM)
- 2 KBytes On-Chip Extension RAM (XRAM)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-Bit or 16-Bit External Data Bus
- Multiplexed or Demultiplexed External Address/Data Buses
- Five Programmable Chip-Select Signals
- Hold- and Hold-Acknowledge Bus Arbitration Support
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 50 ns
- 16-Channel 10-bit A/D Converter with 9.7µs Conversion Time
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with 5 Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- On-Chip CAN Interface with 15 Message Objects (Full-CAN/Basic-CAN, C167CR-LC only)
- Programmable Watchdog Timer
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Supported by a Wealth of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader

This document describes the **SAK-C167CR-LC** and the **SAK-C167SR-LC**.
For simplicity all versions are referred to by the term **C167xR-LC** throughout this document.

Introduction

The C167xR-LC is a derivative of the Siemens C16x Family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 10 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. It also provides on-chip high-speed RAM and clock generation via PLL.

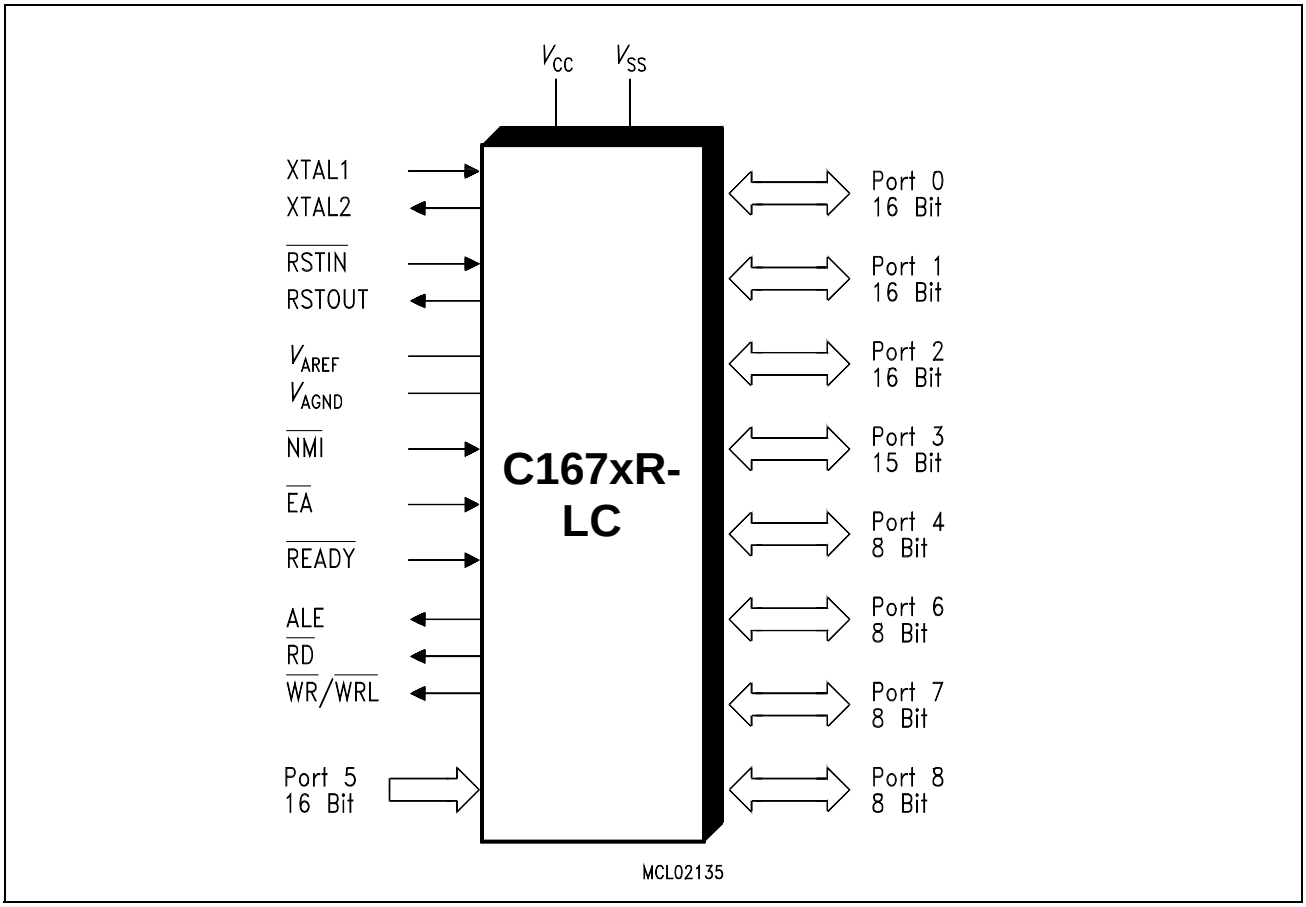

Figure 1
Logic Symbol

Ordering Information

Type	Ordering Code	Wafers	Function
SAK-C167CR-LC	Q67120-C1089	Whole	16-bit microcontroller with 2*2 KByte RAM Temperature range -40 to +125 °C
SAK-C167CR-LC	Q67120-C1028	Sawn	16-bit microcontroller with 2*2 KByte RAM Temperature range -40 to +125 °C
SAK-C167SR-LC	Q67120-C1080	Sawn	16-bit microcontroller with 2*2 KByte RAM Temperature range -40 to +125 °C

Pad Configuration
(top view)

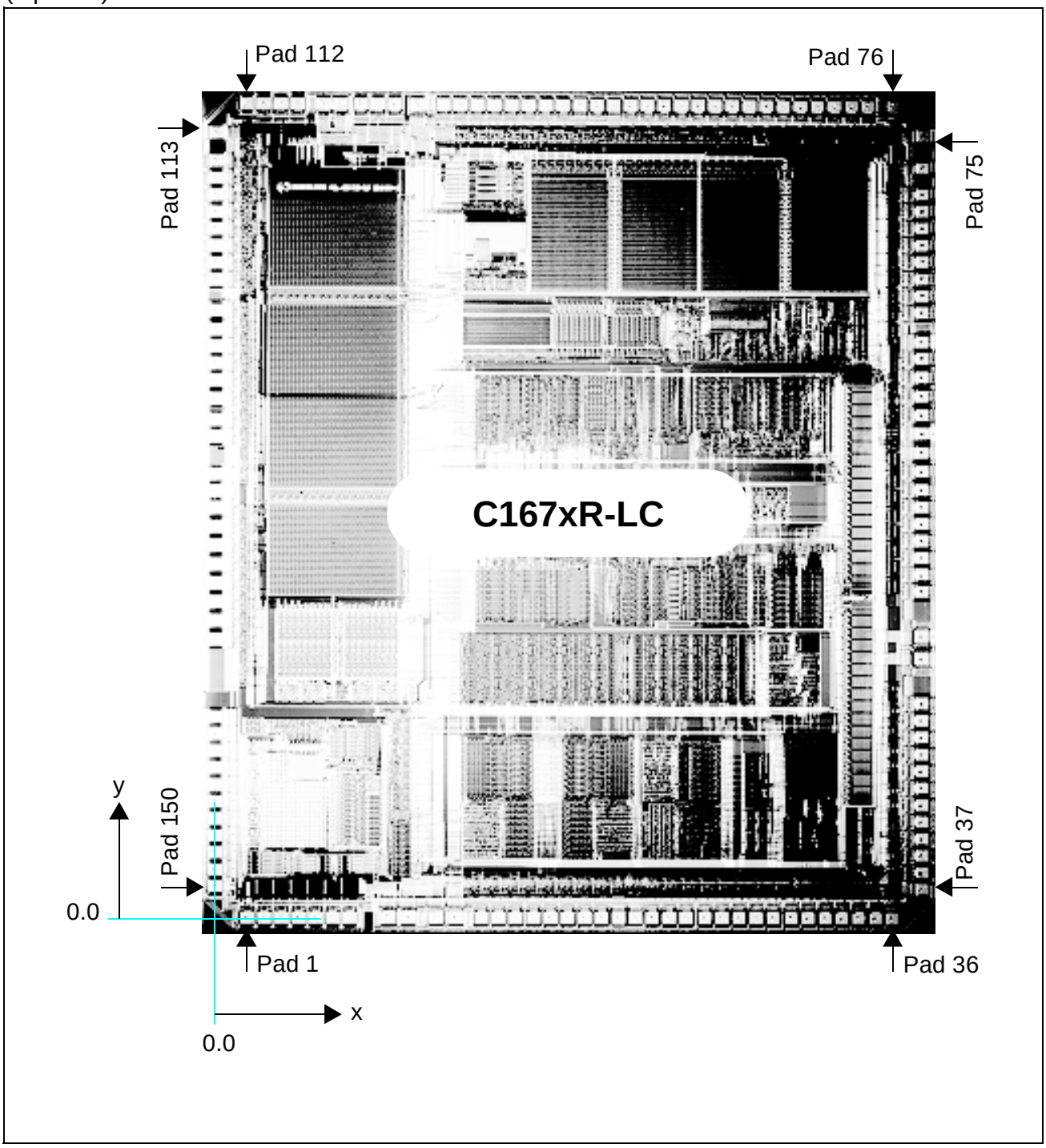

Figure 2

Pad Definitions and Functions

Symbol	Pad Num.	Input Outp.	Position [µm] x	y	Function
V_{AGND}	1	-	293	0	Reference ground for the A/D converter.
P5.10	2	I	451	0	Port 5 input, analog input AN10, ext.up/down T6EUD.
P5.11	3	I	609	0	Port 5 input, analog input AN11, ext.up/down T5EUD.
P5.12	4	I	766	0	Port 5 input, analog input AN12, timer input T6IN.
P5.13	5	I	924	0	Port 5 input, analog input AN13, timer input T5IN.
P5.14	6	I	1082	0	Port 5 input, analog input AN14, ext.up/down T4EUD.
P5.15	7	I	1240	0	Port 5 input, analog input AN15, ext.up/down T2EUD.
V_{SS}	8	-	1604	0	Digital Ground.
V_{SS}	9	-	1788	0	Digital Ground.
V_{CC}	10	-	2046	0	Digital Supply Voltage.
V_{CC}	11	-	2226	0	Digital Supply Voltage.
P2.0	12	I/O	2463	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC0IO.
P2.1	13	I/O	2621	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC1IO.
P2.2	14	I/O	2778	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC2IO.
P2.3	15	I/O	2945	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC3IO.
P2.4	16	I/O	3103	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC4IO.
P2.5	17	I/O	3261	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC5IO.
P2.6	18	I/O	3419	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC6IO.
P2.7	19	I/O	3577	0	Port 2 input/output (open drain, special threshold), Capture-Input/Compare-Output CC7IO.
V_{SS}	20	-	3735	0	Digital Ground.
V_{CC}	21	-	3893	0	Digital Supply Voltage.
P2.8	22	I/O	4050	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC8IO, Fast Interrupt EX0IN.
P2.9	23	I/O	4208	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC9IO, Fast Interrupt EX1IN.
P2.10	24	I/O	4366	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC10IO, Fast Interrupt EX2IN.

Pad Definitions and Functions (cont'd)

Symbol	Pad Num.	Input Outp.	Position [µm] x	y	Function
P2.11	25	I/O	4542	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC11IO, Fast Interrupt EX3IN.
P2.12	26	I/O	4699	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC12IO, Fast Interrupt EX4IN.
P2.13	27	I/O	4857	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC13IO, Fast Interrupt EX5IN.
P2.14	28	I/O	5015	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC14IO, Fast Interrupt EX6IN.
P2.15	29	I/O	5173	0	Port 2 input/output (open drain, special threshold), Capt. Input/Comp. Output CC15IO, Fast Interrupt EX7IN, Timer T7 input T7IN.
P3.0	30	I/O	5340	0	Port 3 input/output (open drain, special threshold), Timer T0 Input T0IN.
P3.1	31	I/O	5498	0	Port 3 input/output (open drain, special threshold), Timer T6 Toggle Latch Output T6OUT.
P3.2	32	I/O	5656	0	Port 3 input/output (open drain, special threshold), CAPREL Capture Input CAPIN.
P3.3	33	I/O	5814	0	Port 3 input/output (open drain, special threshold), Timer T3 Toggle Latch Output T3OUT.
P3.4	34	I/O	5971	0	Port 3 input/output (open drain, special threshold), Timer T3 ext.up/down T3EUD.
P3.5	35	I/O	6129	0	Port 3 input/output (open drain, special threshold), Timer T4 Input T4IN.
V_{SS}	36	-	6287	0	Digital Ground.
V_{CC}	37	-	6564	277	Digital Supply Voltage.
P3.6	38	I/O	6564	435	Port 3 input/output (open drain, special threshold), Timer T3 Input T3IN.
P3.7	39	I/O	6564	593	Port 3 input/output (open drain, special threshold), Timer T2 Input T2IN.
P3.8	40	I/O	6564	751	Port 3 input/output (open drain, special threshold), SSC Master-Rec./Slave-Transmit I/O MRST.
P3.9	41	I/O	6564	909	Port 3 input/output (open drain, special threshold), SSC Master-Transmit/Slave-Rec. O/I MTSR.
P3.10	42	I/O	6564	1067	Port 3 input/output (open drain, special threshold), ASC0 Clock/Data Output (Asyn./Syn.) T×D0.

Pad Definitions and Functions (cont'd)

Symbol	Pad Num.	Input Outp.	Position [µm] x	y	Function
P3.11	43	I/O	6564	1225	Port 3 input/output (open drain, special threshold), ASC0 Data Input (Asyn.) or I/O (Syn.) R×D0.
P3.12	44	I/O	6564	1383	Port 3 input/output (open drain, special threshold).
	45	O	6564	1540	High Byte Enable $\overline{\text{BHE}}$, High Byte Write Strobe $\overline{\text{WRH}}$.
P3.13	46	I/O	6564	1698	Port 3 input/output (open drain, special threshold), SSC Master Clock Outp./Slave Clock Input SCLK.
P3.15	47	I/O	6564	1856	Port 3 input/output (open drain, special threshold).
	48	I/O	6564	2014	System Clock Output (=CPU Clock) CLKOUT.
V_{CC}	49	-	6564	2433	Digital Supply Voltage.
V_{SS}	50	-	6564	2643	Digital Ground.
P4.0	51	I/O	6564	3062	Port 4 input/output, Segment Address Line A16.
P4.1	52	I/O	6564	3220	Port 4 input/output, Segment Address Line A17.
P4.2	53	I/O	6564	3378	Port 4 input/output, Segment Address Line A18.
P4.3	54	I/O	6564	3693	Port 4 input/output, Segment Address Line A19.
P4.4	55	I/O	6564	3062	Port 4 input/output, Segment Address Line A20.
P4.5	56	I/O	6564	3851	Port 4 input/output, Segment Address Line A21, CAN Receive Data Input CAN_RxD.
P4.6	57	I/O	6564	4009	Port 4 input/output, Segment Address Line A22 CAN Transmit Data Output CAN_TxD.
P4.7	58	I/O	6564	4184	Port 4 input/output, Segment Address Line A23.
V_{CC}	59	-	6564	4360	Digital Supply Voltage.
V_{SS}	60	-	6564	4535	Digital Ground.
$\overline{\text{RD}}$	61	O	6564	4710	External Memory Read Strobe $\overline{\text{RD}}$.
$\overline{\text{WR}}$($\overline{\text{L}}$)	62	O	6564	4885	External Memory Write (Low) Strobe $\overline{\text{WR}}$ ($\overline{\text{WRL}}$).
$\overline{\text{READY}}$	63	I	6564	5060	Ready Input.
ALE	64	O	6564	5236	Address Latch Enable Output.
$\overline{\text{EA}}$	65	I	6564	5394	External Access Enable pin.
P0L.0	66	I/O	6564	5664	PORT0 input/output, Address/Data Line AD0.
P0L.1	67	I/O	6564	5822	PORT0 input/output, Address/Data Line AD1.
P0L.2	68	I/O	6564	5980	PORT0 input/output, Address/Data Line AD2.
P0L.3	69	I/O	6564	6138	PORT0 input/output, Address/Data Line AD3.
P0L.4	70	I/O	6564	6295	PORT0 input/output, Address/Data Line AD4.
P0L.5	71	I/O	6564	6453	PORT0 input/output, Address/Data Line AD5.

Pad Definitions and Functions (cont'd)

Symbol	Pad Num.	Input Outp.	Position [µm] x	y	Function
P0L.6	72	I/O	6564	6611	PORT0 input/output, Address/Data Line AD6.
P0L.7	73	I/O	6564	6769	PORT0 input/output, Address/Data Line AD7.
P0H.0	74	I/O	6564	7014	PORT0 input/output, Address/Data Line AD8.
V_{CC}	75	-	6564	7313	Digital Supply Voltage.
V_{SS}	76	-	6052	7590	Digital Ground.
P0H.1	77	I/O	6564	7590	PORT0 input/output, Address/Data Line AD9.
P0H.2	78	I/O	5894	7590	PORT0 input/output, Address/Data Line AD10.
P0H.3	79	I/O	5736	7590	PORT0 input/output, Address/Data Line AD11.
P0H.4	80	I/O	5578	7590	PORT0 input/output, Address/Data Line AD12.
P0H.5	81	I/O	5420	7590	PORT0 input/output, Address/Data Line AD13.
P0H.6	82	I/O	5262	7590	PORT0 input/output, Address/Data Line AD14.
P0H.7	83	I/O	5104	7590	PORT0 input/output, Address/Data Line AD15.
P1L.0	84	I/O	4946	7590	PORT1 input/output, Address Line A0.
P1L.1	85	I/O	4788	7590	PORT1 input/output, Address Line A1.
P1L.2	86	I/O	4630	7590	PORT1 input/output, Address Line A2.
P1L.3	87	I/O	4472	7590	PORT1 input/output, Address Line A3.
P1L.4	88	I/O	4314	7590	PORT1 input/output, Address Line A4.
P1L.5	89	I/O	4157	7590	PORT1 input/output, Address Line A5.
P1L.6	90	I/O	3999	7590	PORT1 input/output, Address Line A6.
P1L.7	91	I/O	3841	7590	PORT1 input/output, Address Line A7.
V_{CC}	92	-	3683	7590	Digital Supply Voltage.
$\overline{\text{XP1\_EN}}$	93	I	3525	7590	CAN module enable input, must be connected to V_{SS} (for the C167CR-LC) or to V_{CC} (for the C167SR-LC).
V_{SS}	94	-	3367	7590	Digital Ground.
P1H.0	95	I/O	3209	7590	PORT1 input/output, Address Line A8.
P1H.1	96	I/O	3051	7590	PORT1 input/output, Address Line A9.
P1H.2	97	I/O	2893	7590	PORT1 input/output, Address Line A10.
P1H.3	98	I/O	2735	7590	PORT1 input/output, Address Line A11.
P1H.4	99	I/O	2577	7590	PORT1 input/output, Addr. Line A12, Capt. Input CC24.
P1H.5	100	I/O	2419	7590	PORT1 input/output, Addr. Line A13, Capt. Input CC25.
P1H.6	101	I/O	2262	7590	PORT1 input/output, Addr. Line A14, Capt. Input CC26.
P1H.7	102	I/O	2104	7590	PORT1 input/output, Addr. Line A15, Capt. Input CC27.

Pad Definitions and Functions (cont'd)

Symbol	Pad Num.	Input Outp.	Position [µm] x	y	Function
V_{CC}	103	-	1867	7590	Digital Supply Voltage.
TLRON	104	I	1650	7590	Must be connected to V_{SS}.
XTAL2	105	O	1492	7590	Output of the oscillator amplifier circuit.
XTAL1	106	I	1334	7590	Input to oscillator amplifier and internal clock generator.
V_{SS}	107	-	1146	7590	Digital Ground.
V_{SS}	108	-	988	7590	Digital Ground.
$\overline{\text{RSTIN}}$	109	I	751	7590	Reset Input with Schmitt-Trigger characteristics.
$\overline{\text{RSTOUT}}$	110	O	593	7590	Internal Reset Indication Output.
$\overline{\text{NMI}}$	111	I	435	7590	Non-Maskable Interrupt Input.
V_{SS}	112	-	277	7590	Digital Ground.
V_{CC}	113	-	0	7313	Digital Supply Voltage.
P6.0	114	I/O	0	7051	Port 6 input/output, Chip Select 0 Output $\overline{\text{CS0}}$.
P6.1	115	I/O	0	6893	Port 6 input/output, Chip Select 1 Output $\overline{\text{CS1}}$.
P6.2	116	I/O	0	6735	Port 6 input/output, Chip Select 2 Output $\overline{\text{CS2}}$.
P6.3	117	I/O	0	6577	Port 6 input/output, Chip Select 3 Output $\overline{\text{CS3}}$.
P6.4	118	I/O	0	6419	Port 6 input/output, Chip Select 4 Output $\overline{\text{CS4}}$.
P6.5	119	I/O	0	6261	Port 6 input/output, External Hold Request Input $\overline{\text{HOLD}}$.
P6.6	120	I/O	0	6103	Port 6 input/output, External Hold Ackn. Output $\overline{\text{HLDA}}$.
P6.7	121	I/O	0	5946	Port 6 input/output, Bus Request Output $\overline{\text{BREQ}}$.
P8.0	122	I/O	0	5658	Port 8 input/output, Capt.-Input/Comp.-Output CC16IO.
P8.1	123	I/O	0	5483	Port 8 input/output, Capt.-Input/Comp.-Output CC17IO.
P8.2	124	I/O	0	5325	Port 8 input/output, Capt.-Input/Comp.-Output CC18IO.
P8.3	125	I/O	0	5167	Port 8 input/output, Capt.-Input/Comp.-Output CC19IO.
P8.4	126	I/O	0	5009	Port 8 input/output, Capt.-Input/Comp.-Output CC20IO.
P8.5	127	I/O	0	4834	Port 8 input/output, Capt.-Input/Comp.-Output CC21IO.
P8.6	128	I/O	0	4641	Port 8 input/output, Capt.-Input/Comp.-Output CC22IO.
P8.7	129	I/O	0	4483	Port 8 input/output, Capt.-Input/Comp.-Output CC23IO.
V_{CC}	130	-	0	4135	Digital Supply Voltage.
V_{SS}	131	-	0	3978	Digital Ground.
P7.0	132	I/O	0	3820	Port 7 input/output, (open drain, special threshold), PWM Channel Output POUT0.

Pad Definitions and Functions (cont'd)

Symbol	Pad Num.	Input Outp.	Position [µm] x	y	Function
P7.1	133	I/O	0	3644	Port 7 input/output, (open drain, special threshold), PWM Channel Output POUT1.
P7.2	134	I/O	0	3469	Port 7 input/output, (open drain, special threshold), PWM Channel Output POUT2.
P7.3	135	I/O	0	3294	Port 7 input/output, (open drain, special threshold), PWM Channel Output POUT3.
P7.4	136	I/O	0	3119	Port 7 input/output, (open drain, special threshold), Capt.-Input/Comp.-Output CC28IO.
P7.5	137	I/O	0	2944	Port 7 input/output, (open drain, special threshold), Capt.-Input/Comp.-Output CC29IO.
P7.6	138	I/O	0	2768	Port 7 input/output, (open drain, special threshold), Capt.-Input/Comp.-Output CC30IO.
P7.7	139	I/O	0	2593	Port 7 input/output, (open drain, special threshold), Capt.-Input/Comp.-Output CC31IO.
P5.0	140	I	0	1872	Port 5 input, analog input AN0.
P5.1	141	I	0	1714	Port 5 input, analog input AN1.
P5.2	142	I	0	1556	Port 5 input, analog input AN2.
P5.3	143	I	0	1398	Port 5 input, analog input AN3.
P5.4	144	I	0	1240	Port 5 input, analog input AN4.
P5.5	145	I	0	1082	Port 5 input, analog input AN5.
P5.6	146	I	0	924	Port 5 input, analog input AN6.
P5.7	147	I	0	766	Port 5 input, analog input AN7.
P5.8	148	I	0	609	Port 5 input, analog input AN8.
P5.9	149	I	0	451	Port 5 input, analog input AN9.
V_{AREF}	150	-	0	293	Reference voltage for the A/D converter.

Note: All V_{SS} pads and all V_{CC} pads must be connected to the system ground and the power supply, respectively.
The pad definitions and locations in this table are only valid for the indicated device and design step.

Functional Description

As the standard packaged devices are made from this silicon the C167xR-LC dies provide exactly the same functionality and behaviour. Also the DC characteristics and AC characteristics are compatible with those of the packaged devices.

For a description of the functionality and the DC and AC parameters please refer to the following documents (or later versions thereof):

- C167SR Data Sheet 06.95
- C167CR Data Sheet 06.95
- C167 Derivatives User's Manual Version 2.0

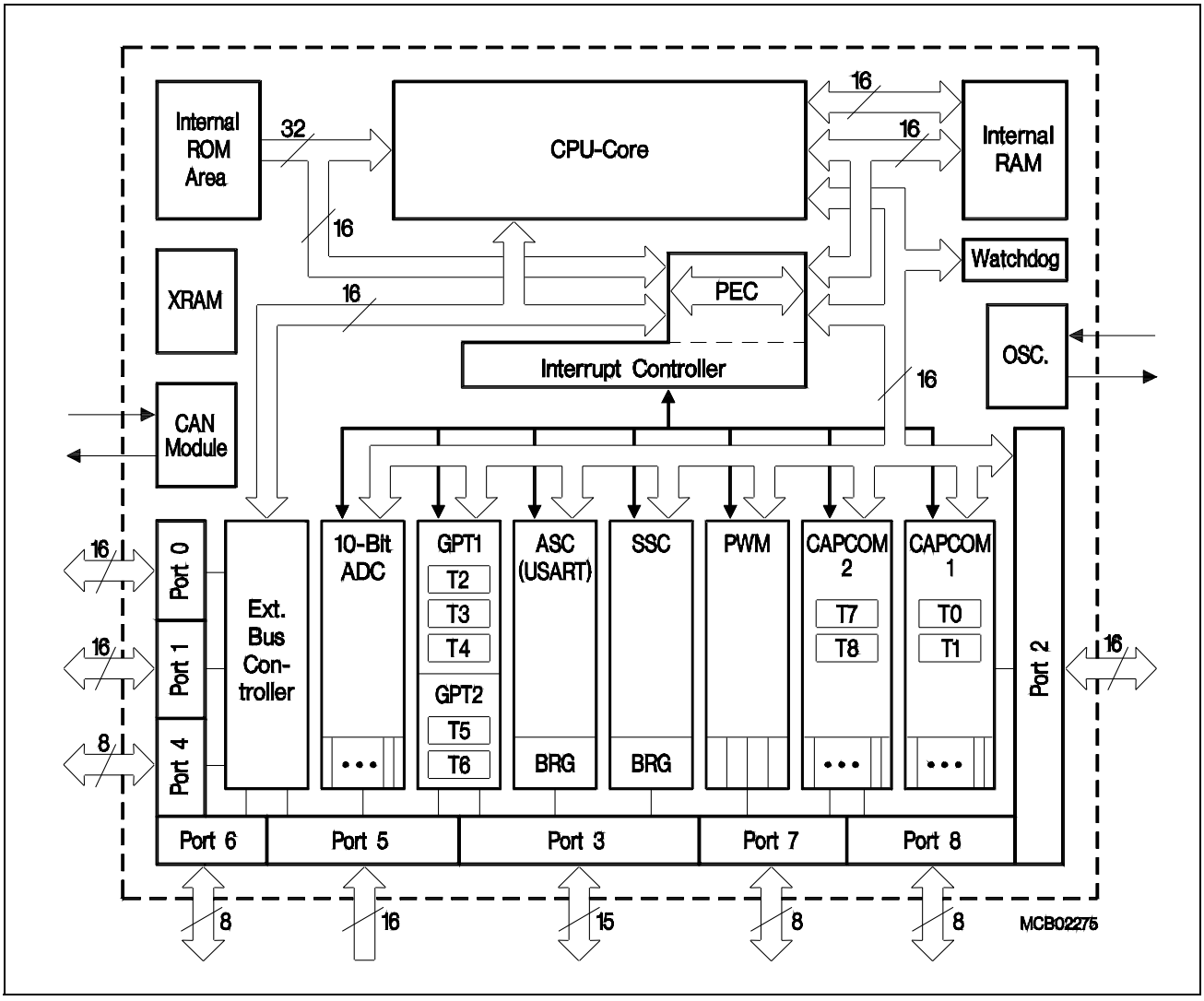

Figure 3
Block Diagram

Absolute Maximum Ratings

Chip temperature under bias (T_D):
SAF-C167xR-LC ..... –40 to +85 °C
SAK-C167xR-LC ..... –40 to +125 °C
Storage temperature (T_{ST}) ..... – 65 to +150 °C
Voltage on V_{CC} pads with respect to ground (V_{SS}) ..... –0.5 to +6.5 V
Voltage on any pad with respect to ground (V_{SS}) ..... –0.5 to V_{CC} +0.5 V
Input current on any pad during overload condition ..... –10 to +10 mA
Absolute sum of all input currents during overload condition ..... |100 mA|

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{CC} or V_{IN}<V_{SS}) the voltage on pads with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

Operating Conditions

The operating conditions for the C167xR-LC are identical with the conditions for the packaged parts. Please refer to the mentioned data sheets.

Note: Temperature specifications refer to the carrier side of the die (T_D).

Storage Conditions

The C167xR-LC dies may be stored for a certain time under the conditions described below.

Bare Die Storage Conditions and Duration

Packing	Environment	Temperature	Relative Humidity	Storage Time
Vacuum pack	Air	15...30 °C	< 60 %	< 4 Months

Chip Outline

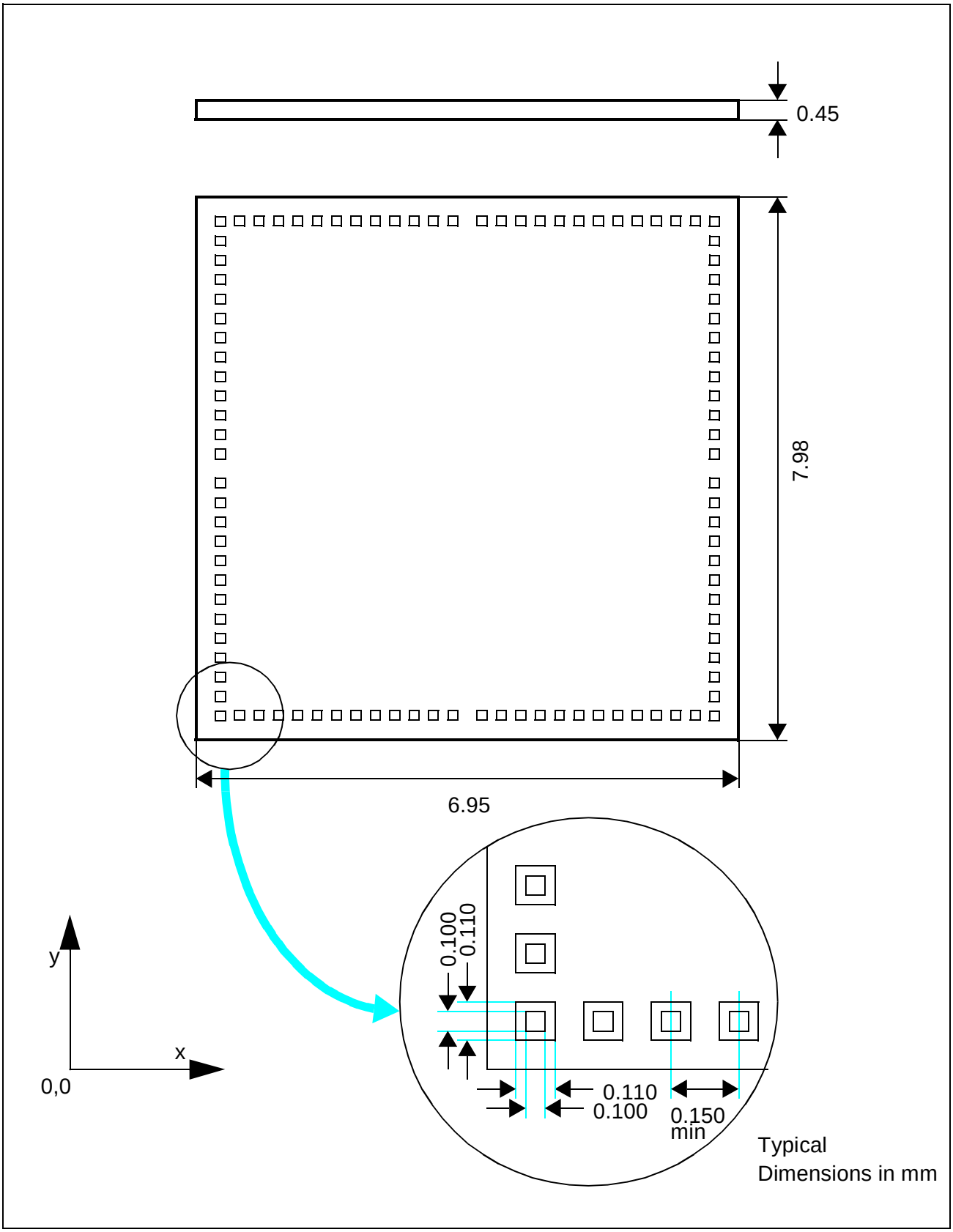

Figure 4

Wafer Characteristics

Item	Characteristic
Chips per wafer	258 (geometrically)
Metallization layers	2
Metallization material	AlSiCu (Al 98.5% - SI 1% - Cu 0.5%)
Metallization thickness	Met1: 800 nm, Met2: 1000 nm
Metallization barrier material	Ti/TiN
Metallization isolation	Oxide
Metallization material on pads	AlSiCu (Al 98.5% - SI 1% - Cu 0.5%)
Passivation	Oxide (300 nm) + nitride (550 nm), polyimid
Backside metallization	None (silicon)
Inkdot diameter	1.0-1.3 mm typical

The wafers are glued to a plastic tape which is fixed within a plastic ring (see figure below). Wafers can be shipped in one piece or sawn into individual dies.

Wafer Outline

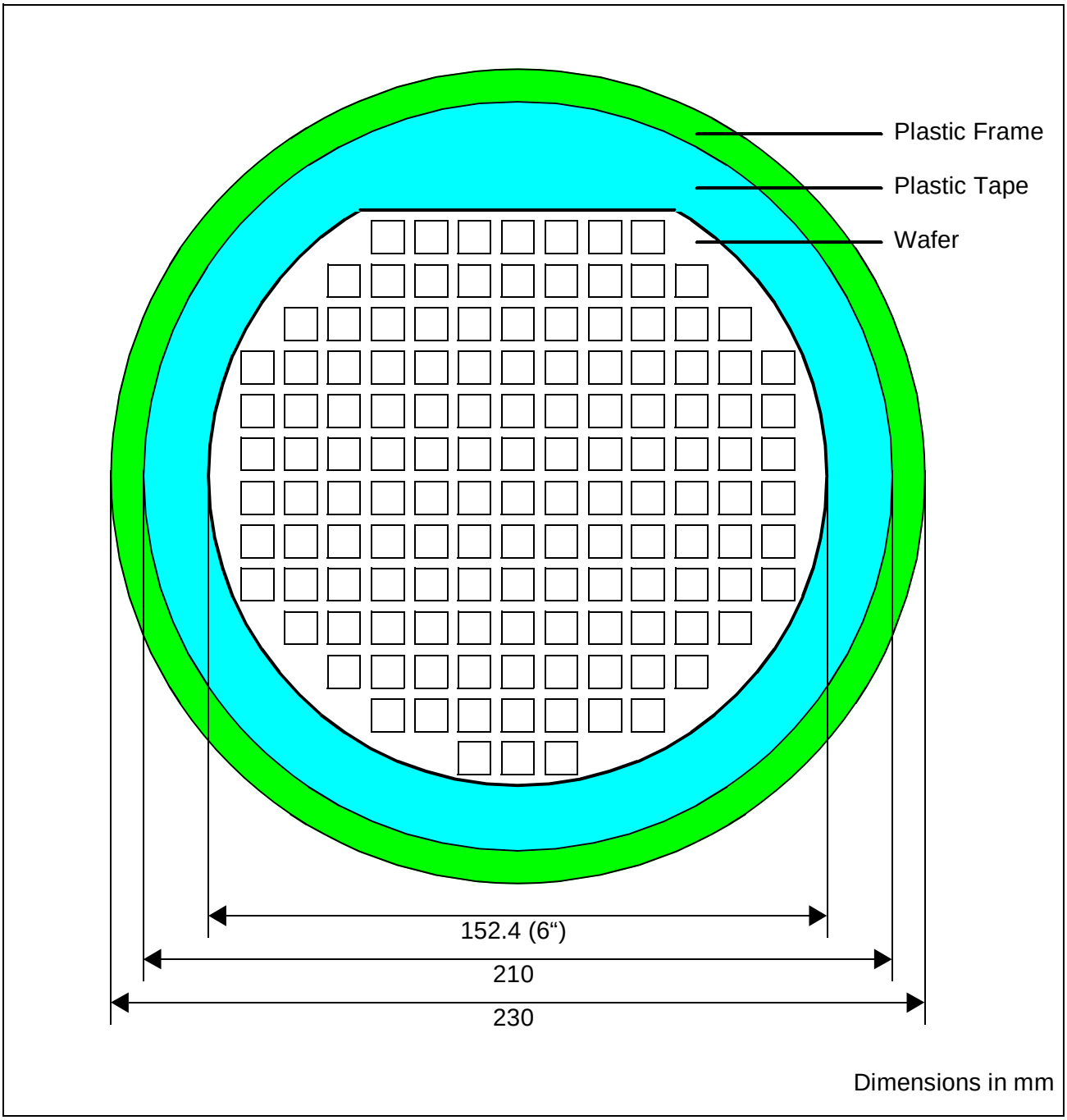

Figure 5