SIEMENS

Microcomputer Components

16-Bit CMOS Single-Chip Microcontroller
25 MHz

C165

Specification 07.95 Preliminary

C165 Revision History:	07.95 Original Version 25 MHz
Previous Releases:	09.94 (20 MHz)
Page	**Subjects (changes since last revision)**
8	External Clock Drive Specification changed.
9	t_6, t_{14}, t_{15}, t_{16}, t_{17} updated.
10	t_{22} updated.
12	t_6, t_{14}, t_{15}, t_{16}, t_{17}, t_{22} updated.
13	t_{55} updated.
14	t_{35}, t_{36}, t_{59}, t_{16}, t_{17}, t_{22} updated.

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SIEMENS

C16x-Family of C165
High-Performance CMOS 16-Bit Microcontrollers

Preliminary
C165 16-Bit Microcontroller, 25 MHz

- High Performance 16-bit CPU with 4-Stage Pipeline
- 80 ns Instruction Cycle Time at 25-MHz CPU Clock
- 400 ns Multiplication (16 × 16 bits), 800 ns Division (32 / 16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Up to 16 MBytes Linear Address Space for Code and Data
- 2 KBytes On-Chip RAM
- 4 KBytes On-Chip ROM (RM types only)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-Bit or 16-Bit External Data Bus
- Multiplexed or Demultiplexed External Address/Data Buses
- Five Programmable Chip-Select Signals
- Hold- and Hold-Acknowledge Bus Arbitration Support
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 28 Sources, Sample-Rate down to 40 ns
- Two Multi-Functional General Purpose Timer Units with 5 Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- Programmable Watchdog Timer
- Up to 77 General Purpose I/O Lines
- Supported by a Wealth of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin MQFP Package (EIAJ)
- 100-Pin TQFP Package (Thin QFP)

This document describes specific items relevant for operation at 25 MHz.
For functional descriptions please refer to the standard C165 data sheet.

This document describes the **SAB-C165-L25M,** the **SAB-C165-L25F,** the **SAB-C165-R25M** and the **SAB-C165-R25F**.
For simplicity all versions are referred to by the term **C165** throughout this document.

Ordering Information:

Type	Ordering Code	Package	Function
SAB-C165-R25M	Q67121-D...	P-MQFP-100-2	16-bit microcontroller with 2 KByte RAM and 4 KByte ROM Temperature range 0 to +70 °C
SAB-C165-L25M	Q67121-C1005	P-MQFP-100-2	16-bit microcontroller with 2 KByte RAM Temperature range 0 to +70 °C
SAB-C165-R25F	Q67121-D...	P-TQFP-100-3	16-bit microcontroller with 2 KByte RAM and 4 KByte ROM Temperature range 0 to +70 °C
SAB-C165-L25F	Q67121-C1004	P-TQFP-100-3	16-bit microcontroller with 2 KByte RAM Temperature range 0 to +70 °C

Note: The ordering codes (Q67121-D...) for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

Pin Configuration MQFP Package
(top view)

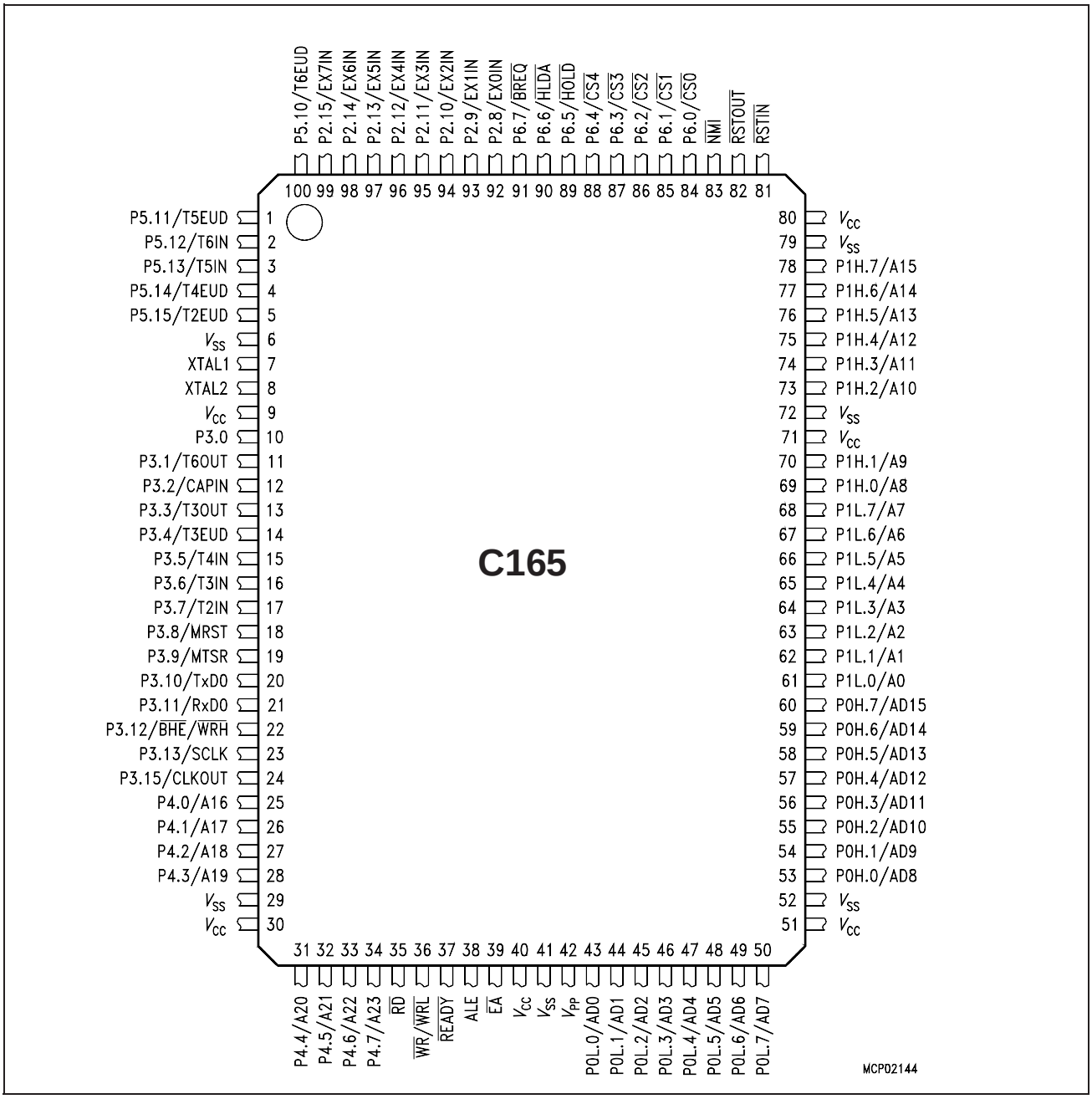

Figure 1

Pin Configuration TQFP Package
(top view)

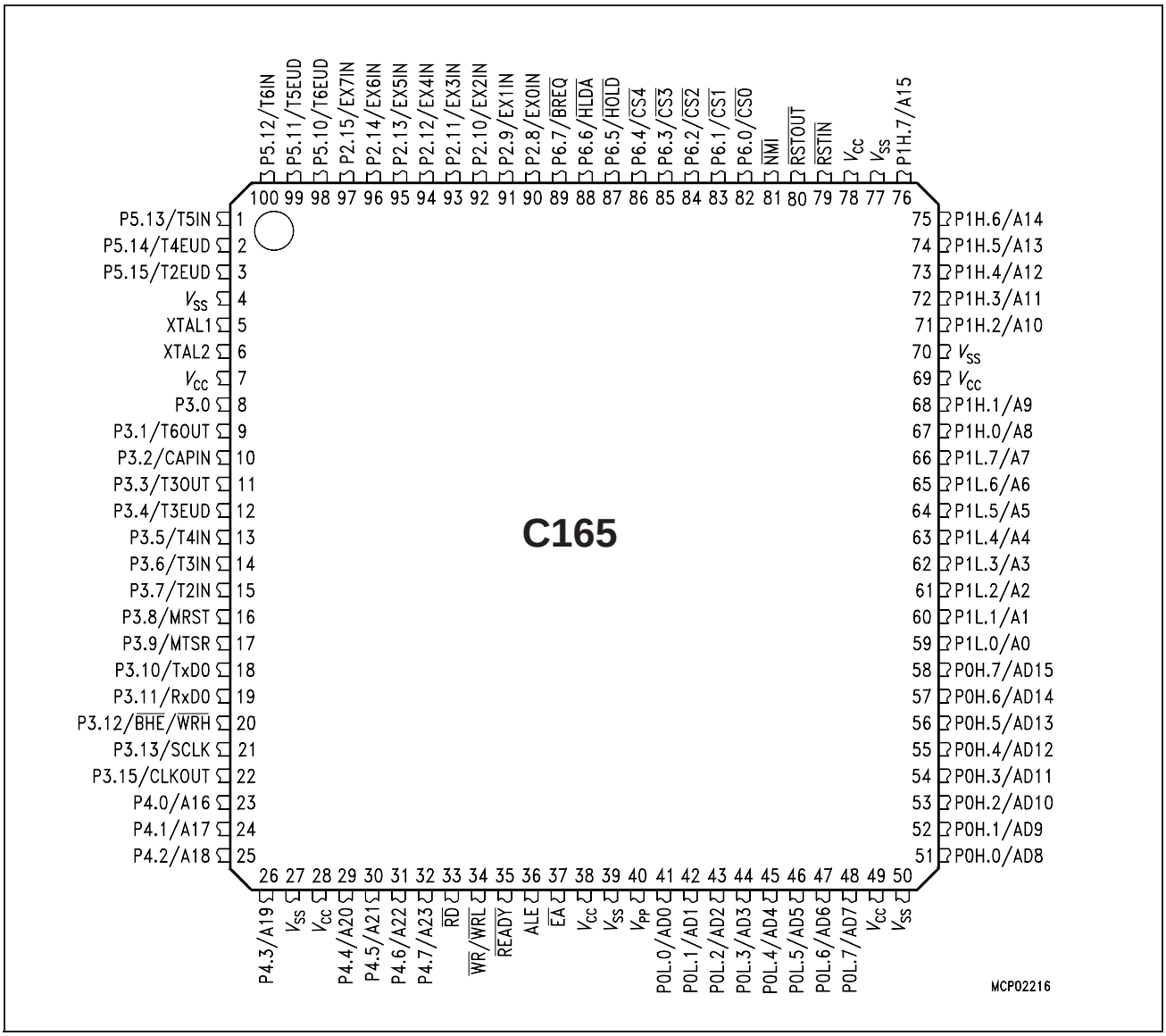

Figure 2

Absolute Maximum Ratings

Ambient temperature under bias (T_A):
SAB-C165-L25M, SAB-C165-R25M, SAB-C165-L25F, SAB-C165-R25F..... 0 to +70 °C
Storage temperature (T_{ST})..... – 65 to +150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... –0.5 to +6.5 V
Voltage on any pin with respect to ground (V_{SS}).....–0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition..... –10 to +10 mA
Absolute sum of all input currents during overload condition .....|100 mA|
Power dissipation..... 1.5 W

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{CC} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C165 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C165 will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C165.

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; f_{CPU} = 25 MHz; Reset active
T_A = 0 to +70 °C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage	V_{IL}	SR	– 0.5	0.2 V_{CC} – 0.1	V	–
Input high voltage (all except $\overline{\text{RSTIN}}$ and XTAL1)	V_{IH}	SR	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage $\overline{\text{RSTIN}}$	V_{IH1}	SR	0.6 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{CC}	V_{CC} + 0.5	V	–

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL} CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	0.9 V_{CC} 2.4	–	V	I_{OH} = – 500 µA I_{OH} = – 2.4 mA
Output high voltage [1] (all other outputs)	V_{OH1} CC	0.9 V_{CC} 2.4	–	V V	I_{OH} = – 250 µA I_{OH} = – 1.6 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0 V < V_{IN} < V_{CC}
Input leakage current (all other)	I_{OZ2} CC	–	±500	nA	0 V < V_{IN} < V_{CC}
$\overline{RSTIN}$ pullup resistor	R_{RST} CC	50	150	kΩ	–
Read/Write inactive current [4]	I_{RWH} [2]	–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [4]	I_{RWL} [3]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [4]	I_{ALEL} [2]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current [4]	I_{ALEH} [3]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current [4]	I_{P6H} [2]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current [4]	I_{P6L} [3]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current [4]	I_{P0H} [2]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L} [3]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{CC}
Pin capacitance [5] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	10 + 4 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [6]
Idle mode supply current	I_{ID}	–	2 + 1.2 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [6]
Power-down mode supply current	I_{PD}	–	100	µA	V_{CC} = 5.5 V [7]

Notes

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2) The maximum current may be drawn while the respective signal line remains inactive.

3) The minimum current must be drawn in order to drive the respective signal line active.

4) This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.

5) Not 100% tested, guaranteed by design characterization.

6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{CCmax} and 25 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

7) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{CC} – 0.1 V to V_{CC}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

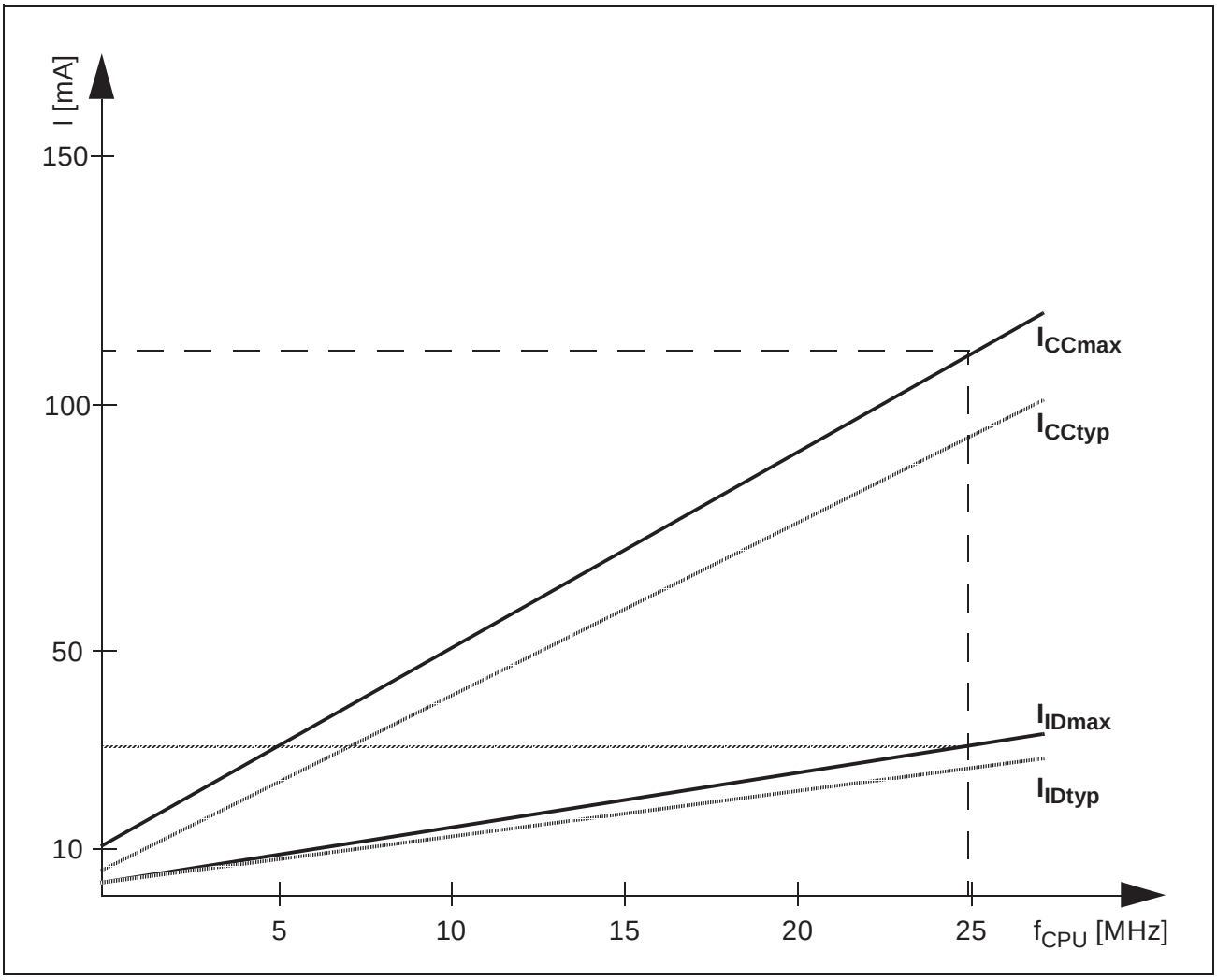

Figure 3
Supply/Idle Current as a Function of Operating Frequency

AC Characteristics
External Clock Drive XTAL1

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	20	20	20	500	ns
High time	t_1	SR	5 [1)]	–	5 [1)]	–	ns
Low time	t_2	SR	5 [1)]	–	5 [1)]	–	ns
Rise time	t_3	SR	–	5 [1)]	–	5 [1)]	ns
Fall time	t_4	SR	–	5 [1)]	–	5 [1)]	ns

[1)] The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

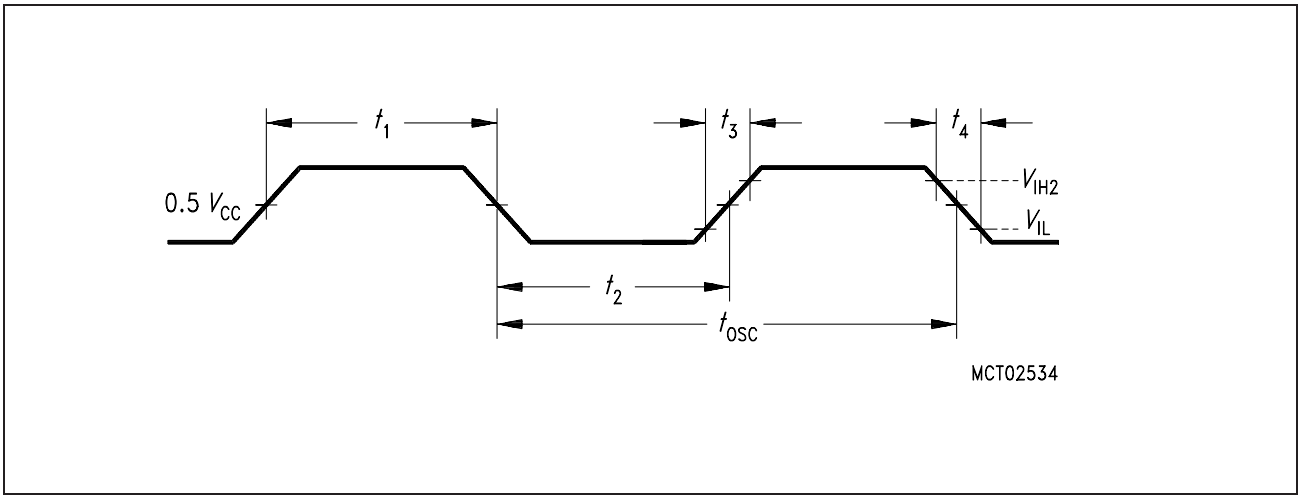

Figure 4
External Clock Drive XTAL1

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL> [1)]
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

AC Characteristics
Multiplexed Bus

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
C_L (for Port 6, $\overline{CS}$) = 100 pF
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (120 ns at 25-MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	2.5 + t_A	–	TCL - 17.5 + t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	5	–	5	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	25	–	TCL + 5	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	25 + t_C	–	2TCL - 15 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	45 + t_C	–	3TCL - 15 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	45 + t_A + t_C	–	3TCL - 15 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	55 + 2t_A + t_C	–	4TCL - 25 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	25 + t_F	–	2TCL - 15 + t_F	ns

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	25 + t_F	–	2TCL - 15 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	25 + t_F	–	2TCL - 15 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	25 + t_F	–	2TCL - 15 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-5 - t_A	10 - t_A	-5 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C+2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40}	CC	45 + t_F	–	3TCL - 15 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	15 + t_A	–	TCL - 5 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-5 + t_A	–	-5 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	20	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	15 + t_C	–	2TCL - 25 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	35 + t_C	–	3TCL - 25 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	25 + t_C	–	2TCL - 15 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$	t_{52}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Address hold after RdCS, WrCS	t_{54}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after WrCS	t_{56}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns

AC Characteristics
Demultiplexed Bus

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
C_L (for Port 6, $\overline{CS}$) = 100 pF
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25-MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	2.5 + t_A	–	TCL - 17.5 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	25 + t_C	–	2TCL - 15 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	45 + t_C	–	3TCL - 15 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	45 + t_A + t_C	–	3TCL - 15 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	55 + 2t_A + t_C	–	4TCL - 25 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay [1)])	t_{20}	SR	–	25 + t_F	–	2TCL - 15 + 2t_A + t_F [1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay [1)])	t_{21}	SR	–	10 + t_F	–	TCL - 10 + 2t_A + t_F [1)]	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-5 - t_A	10 - t_A	-5 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C+2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41}	CC	5 + t_F	–	TCL - 15 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	15 + t_A	–	TCL - 5 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-5 + t_A	–	-5 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	15 + t_C	–	2TCL - 25 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	35 + t_C	–	3TCL - 25 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	40 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	25 + t_C	–	2TCL - 15 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Data float after $\overline{RdCS}$ (no RW-delay)	t_{68}	SR	–	0 + t_F	–	TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{55}	CC	-10 + t_F	–	-10 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{57}	CC	5 + t_F	–	TCL - 15 + t_F	–	ns

[1] RW-delay and t_A refer to the next following bus cycle.

AC Characteristics
CLKOUT and $\overline{\text{READY}}$

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF
C_L (for Port 6, $\overline{\text{CS}}$) = 100 pF

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	15	–	TCL – 5	–	ns
CLKOUT low time	t_{31}	CC	10	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	5	–	5	ns
CLKOUT fall time	t_{33}	CC	–	5	–	5	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	15	–	15	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	5	–	5	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	55	–	2TCL + 15	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	15	–	15	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	5	–	5	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	0 + $2t_A$ + t_C + t_F [2]	0	TCL - 25 + $2t_A$ + t_C + t_F [2]	ns

Notes

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

AC Characteristics
External Bus Arbitration

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
C_L (for Port 6, $\overline{CS}$) = 100 pF

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{HOLD}$ input setup time to CLKOUT	t_{61}	SR	20	–	20	–	ns
CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	t_{62}	CC	–	20	–	20	ns
CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	t_{63}	CC	–	20	–	20	ns
$\overline{CSx}$ release	t_{64}	CC	–	20	–	20	ns
$\overline{CSx}$ drive	t_{65}	CC	-5	25	-5	25	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	-5	25	-5	25	ns

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