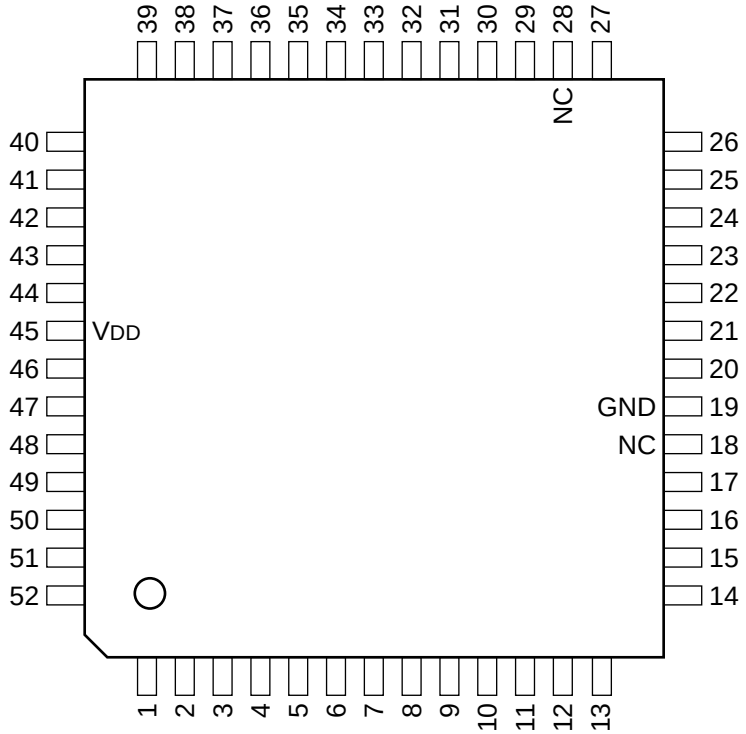
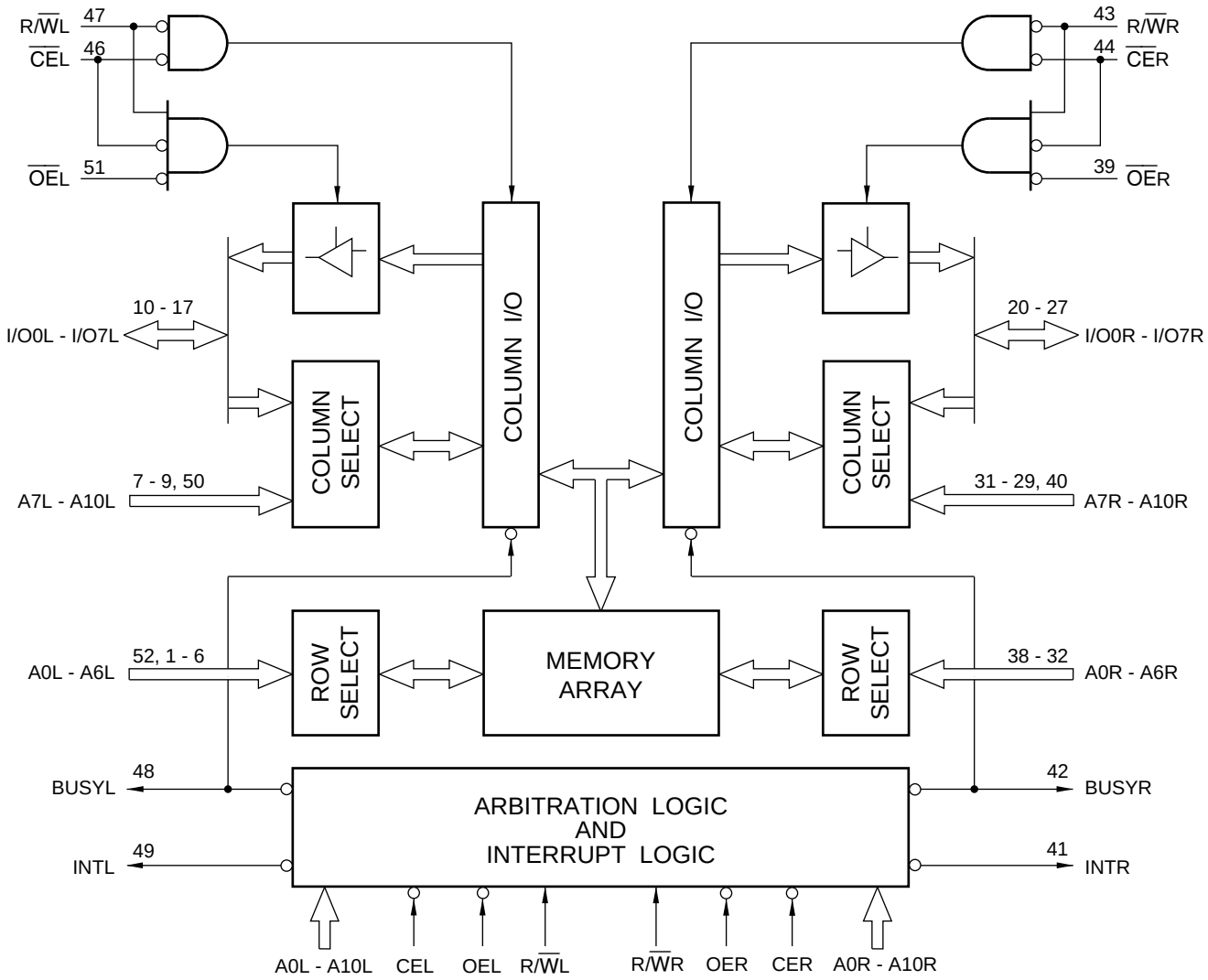
C-MOS 2 K × 8-BIT DUAL-PORT SRAM

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	A1L	14	I/O	I/O4L	27	I/O	I/O7R	40	I	A10R
2	I	A2L	15	I/O	I/O5L	28	—	NC	41	O	$\overline{\text{INT}}$R
3	I	A3L	16	I/O	I/O6L	29	I	A9R	42	O	$\overline{\text{BUSY}}$R
4	I	A4L	17	I/O	I/O7L	30	I	A8R	43	I	R/$\overline{\text{W}}$R
5	I	A5L	18	—	NC	31	I	A7R	44	I	$\overline{\text{CE}}$R
6	I	A6L	19	—	GND	32	I	A6R	45	—	VDD
7	I	A7L	20	I/O	I/O0R	33	I	A5R	46	I	$\overline{\text{CE}}$L
8	I	A8L	21	I/O	I/O1R	34	I	A4R	47	I	R/$\overline{\text{W}}$L
9	I	A9L	22	I/O	I/O2R	35	I	A3R	48	O	$\overline{\text{BUSY}}$L
10	I/O	I/O0L	23	I/O	I/O3R	36	I	A2R	49	O	$\overline{\text{INT}}$L
11	I/O	I/O1L	24	I/O	I/O4R	37	I	A1R	50	I	A10L
12	I/O	I/O2L	25	I/O	I/O5R	38	I	A0R	51	I	$\overline{\text{OE}}$L
13	I/O	I/O3L	26	I/O	I/O6R	39	I	$\overline{\text{OE}}$R	52	I	A0L



INPUT

A0L - A10L, A0R - A10R : ADDRESS
CEL, CER : CHIP SELECT
OEL, OER : OUTPUT ENABLE
R/WL, R/WR : READ/WRITE STROBE

OUTPUT

BUSYL, BUSYR : BUSY FLAG
INTL, INTR : INTERRUPT FLAG

INPUT/OUTPUT

I/O0L - I/O7L, I/O0R - I/O7R : DATA