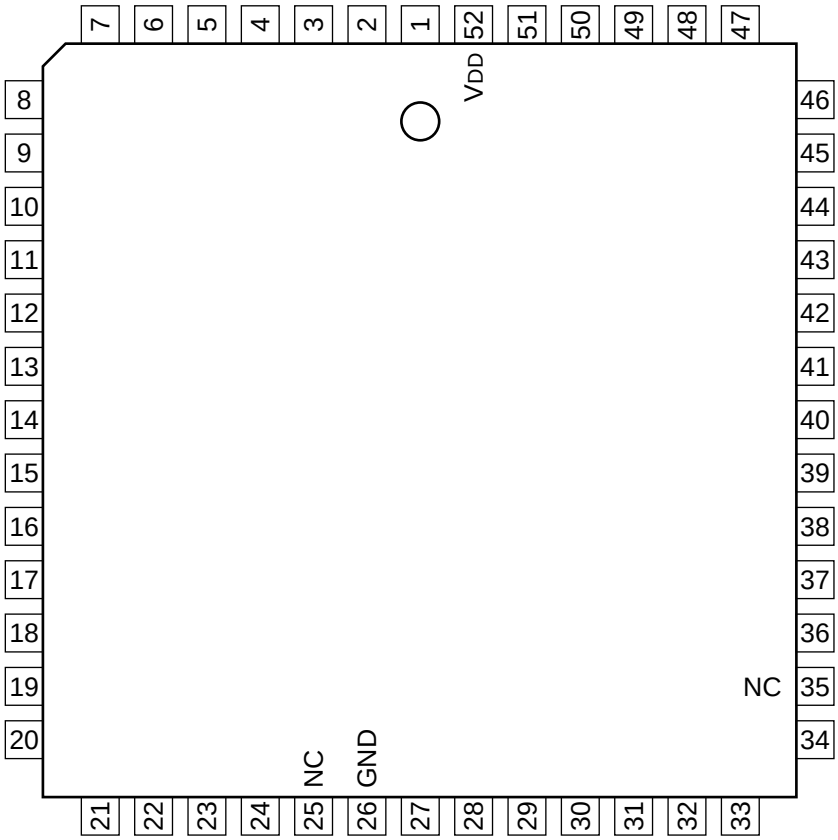
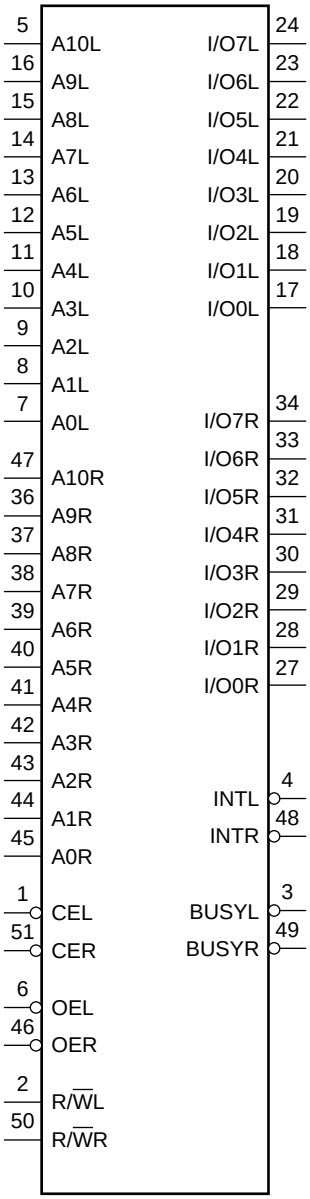
C-MOS (2 K × 8)-BIT DUAL-PORT SRAM

—TOP VIEW—





PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{CE}$L	14	I	A7L	27	I/O	I/O0R	40	I	A5R
2	I	R/$\overline{W}$L	15	I	A8L	28	I/O	I/O1R	41	I	A4R
3	O	$\overline{BUSY}$L	16	I	A9L	29	I/O	I/O2R	42	I	A3R
4	O	$\overline{INT}$L	17	I/O	I/O0L	30	I/O	I/O3R	43	I	A2R
5	I	A10L	18	I/O	I/O1L	31	I/O	I/O4R	44	I	A1R
6	I	$\overline{OE}$L	19	I/O	I/O2L	32	I/O	I/O5R	45	I	A0R
7	I	A0L	20	I/O	I/O3L	33	I/O	I/O6R	46	I	$\overline{OE}$R
8	I	A1L	21	I/O	I/O4L	34	I/O	I/O7R	47	I	A10R
9	I	A2L	22	I/O	I/O5L	35	—	NC	48	O	$\overline{INT}$R
10	I	A3L	23	I/O	I/O6L	36	I	A9R	49	O	$\overline{BUSY}$R
11	I	A4L	24	I/O	I/O7L	37	I	A8R	50	I	R/$\overline{W}$R
12	I	A5L	25	—	NC	38	I	A7R	51	I	$\overline{CE}$R
13	I	A6L	26	—	GND	39	I	A6R	52	—	V_{DD}

INPUT

A0L - A10L, A0R - A10R ; ADDRESS
$\overline{CE}$L, $\overline{CE}$R ; CHIP SELECT
$\overline{OE}$L, $\overline{OE}$R ; OUTPUT ENABLE
R/$\overline{W}$L, R/$\overline{W}$R ; READ/WRITE STROBE

INPUT/OUTPUT

I/O0L - I/O7L, I/O0R - I/O7R ; DATA

OUTPUT

$\overline{BUSY}$L, $\overline{BUCY}$R ; BUSY FLAG
$\overline{INT}$L, $\overline{INT}$R ; INTERRUPT FLAG