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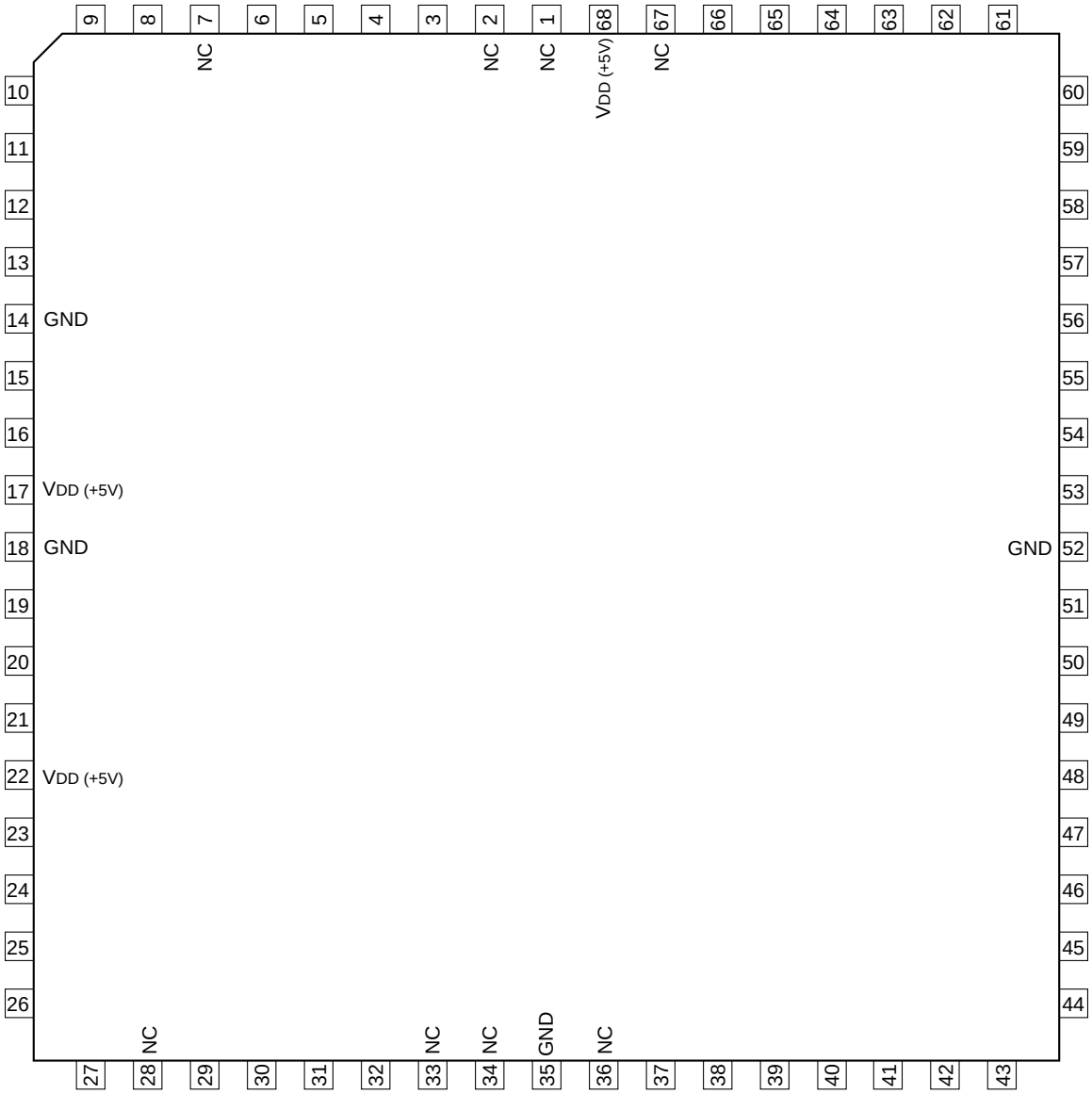
C-MOS 32K (4,096 8)-BIT DUAL-PORT STATIC RAM

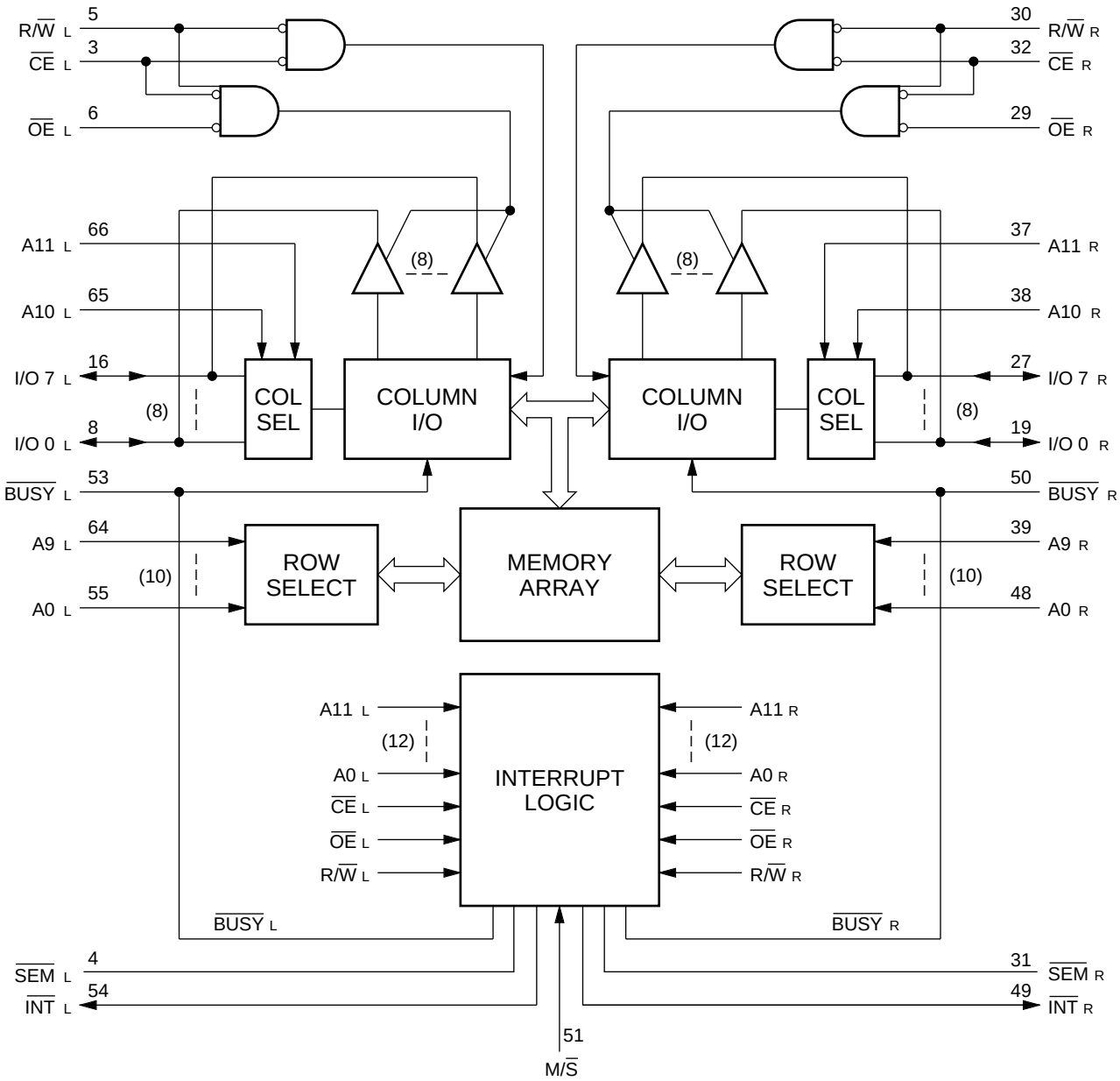
-TOP VIEW-



A0 L/R - A11 L/R ; ADDRESS INPUTS
$\overline{BUSY}$ L/R ; BUSY OUTPUT
$\overline{CE}$ L/R ; CHIP ENABLE INPUT
$\overline{INT}$ L/R ; INTERRUPT OUTPUT
I/O 0 L/R - I/O 7 L/R ; DATA INPUTS / OUTPUTS
M/$\overline{S}$; MAIN/SUB SELECT INPUT
$\overline{OE}$ L/R ; OUTPUT ENABLE INPUT
R/$\overline{W}$ L/R ; READ / WRITE ENABLE INPUT
$\overline{SEM}$ L/R ; SEMAPHORE ENABLE INPUT

(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	18	—	GND	35	—	GND	52	—	GND
2	—	NC	19	I/O	I/O 0 R	36	—	NC	53	O	$\overline{BUSY}$ L
3	I	$\overline{CE}$ L	20	I/O	I/O 1 R	37	I	A11 R	54	I	$\overline{INT}$ L
4	I	$\overline{SEM}$ L	21	I/O	I/O 2 R	38	I	A10 R	55	I	A 0 L
5	I	R/$\overline{W}$ L	22	—	V_{DD}	39	I	A9 R	56	I	A 1 L
6	I	$\overline{OE}$ L	23	I/O	I/O 3 R	40	I	A8 R	57	I	A 2 L
7	—	NC	24	I/O	I/O 4 R	41	I	A7 R	58	I	A 3 L
8	I/O	I/O 0 L	25	I/O	I/O 5 R	42	I	A6 R	59	I	A 4 L
9	I/O	I/O 1 L	26	I/O	I/O 6 R	43	I	A5 R	60	I	A 5 L
10	I/O	I/O 2 L	27	I/O	I/O 7 R	44	I	A4 R	61	I	A 6 L
11	I/O	I/O 3 L	28	—	NC	45	I	A3 R	62	I	A 7 L
12	I/O	I/O 4 L	29	O	$\overline{OE}$ R	46	I	A2 R	63	I	A 8 L
13	I/O	I/O 5 L	30	I	R/$\overline{W}$ R	47	I	A1 R	64	I	A 9 L
14	—	GND	31	I	$\overline{SEM}$ R	48	I	A0 R	65	I	A 10 L
15	I/O	I/O 6 L	32	I	$\overline{CE}$ R	49	O	$\overline{INT}$ R	66	I	A 11 L
16	I/O	I/O 7 L	33	—	NC	50	O	$\overline{BUSY}$ R	67	—	NC
17	—	V_{DD}	34	—	NC	51	I	M/$\overline{S}$	68	—	V_{DD}


R/W L
5
CE L
3
OE L
6
30
R/W R
32
CE R
29
OE R
A11 L
66
A10 L
65
I/O 7 L
16
I/O 0 L
8
(8)
COL SEL
COLUMN I/O
COLUMN I/O
COL SEL
37
A11 R
38
A10 R
27
I/O 7 R
19
I/O 0 R
BUSY L
53
BUSY R
50
A9 L
64
A0 L
55
(10)
ROW SELECT
MEMORY ARRAY
ROW SELECT
39
A9 R
48
A0 R
A11 L
(12)
A0 L
CE L
OE L
R/W L
INTERRUPT LOGIC
A11 R
A0 R
CE R
OE R
R/W R
BUSY L
BUSY R
SEM L
4
INT L
54
31
SEM R
49
INT R
51
M/S