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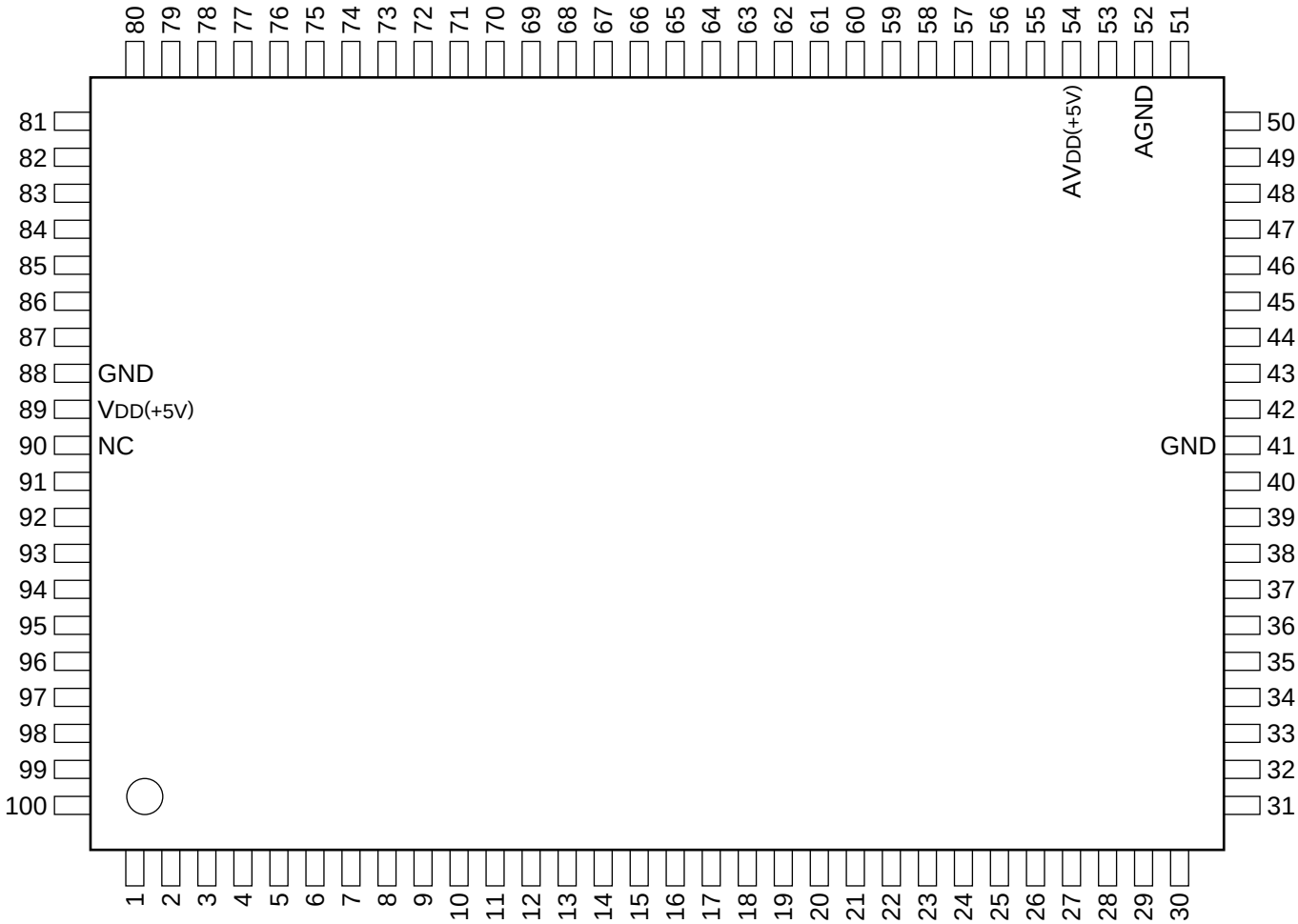
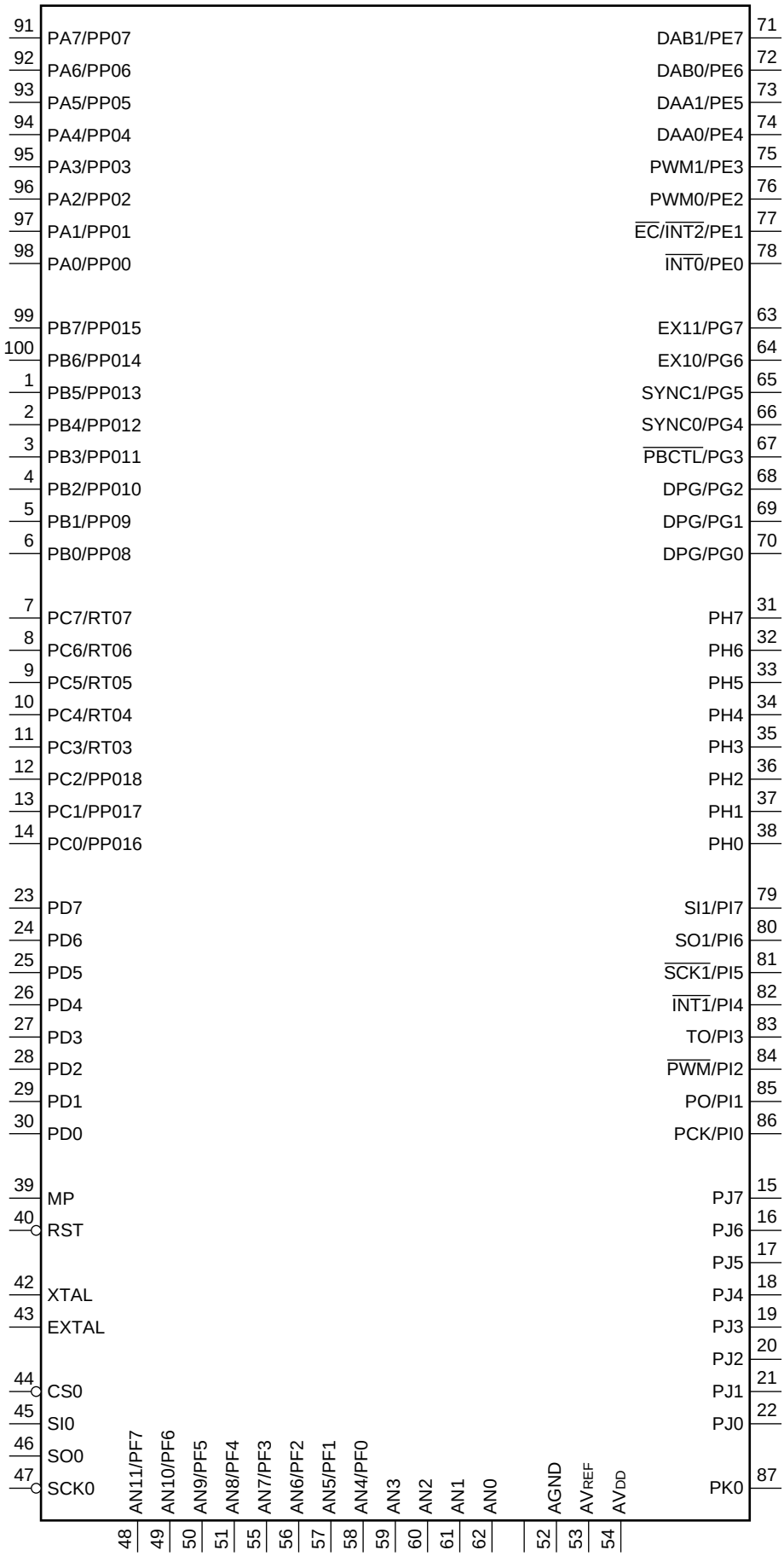
C-MOS 8-BIT 1-CHIP MICROCOMPUTER

–TOP VIEW–




91 PA7/PP07
92 PA6/PP06
93 PA5/PP05
94 PA4/PP04
95 PA3/PP03
96 PA2/PP02
97 PA1/PP01
98 PA0/PP00
99 PB7/PP015
100 PB6/PP014
1 PB5/PP013
2 PB4/PP012
3 PB3/PP011
4 PB2/PP010
5 PB1/PP09
6 PB0/PP08
7 PC7/RT07
8 PC6/RT06
9 PC5/RT05
10 PC4/RT04
11 PC3/RT03
12 PC2/PP018
13 PC1/PP017
14 PC0/PP016
23 PD7
24 PD6
25 PD5
26 PD4
27 PD3
28 PD2
29 PD1
30 PD0
39 MP
40 RST
42 XTAL
43 EXTAL
44 CS0
45 SI0
46 SO0
47 SCK0
71 DAB1/PE7
72 DAB0/PE6
73 DAA1/PE5
74 DAA0/PE4
75 PWM1/PE3
76 PWM0/PE2
77 EC/INT2/PE1
78 INT0/PE0
63 EX11/PG7
64 EX10/PG6
65 SYNC1/PG5
66 SYNC0/PG4
67 PBCTL/PG3
68 DPG/PG2
69 DPG/PG1
70 DPG/PG0
31 PH7
32 PH6
33 PH5
34 PH4
35 PH3
36 PH2
37 PH1
38 PH0
79 SI1/PI7
80 SO1/PI6
81 SCK1/PI5
82 INT1/PI4
83 TO/PI3
84 PWM/PI2
85 PO/PI1
86 PCK/PI0
15 PJ7
16 PJ6
17 PJ5
18 PJ4
19 PJ3
20 PJ2
21 PJ1
22 PJ0
87 PK0
48 AN11/PF7
49 AN10/PF6
50 AN9/PF5
51 AN8/PF4
55 AN7/PF3
56 AN6/PF2
57 AN5/PF1
58 AN4/PF0
59 AN3
60 AN2
61 AN1
62 AN0
52 AGND
53 AVREF
54 AVDD

(V_{DD} = AV_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	PB5/PPO13	26	I/O	PD4	51	I/O	PF4/AN8	76	O	PE2/PWM0
2	O	PB4/PPO12	27	I/O	PD3	52	—	AGND	77	I	PE1/$\overline{EC}$/$\overline{INT2}$
3	O	PB3/PPO11	28	I/O	PD2	53	I	AV_{REF}	78	I	PE0/$\overline{INT0}$
4	O	PB2/PPO10	29	I/O	PD1	54	—	AV_{DD}	79	I/O	PI7/SI1
5	O	PB1/PPO9	30	I/O	PD0	55	I	PF3/AN7	80	I/O	PI6/SO1
6	O	PB0/PPO8	31	I/O	PH7	56	I	PF2/AN6	81	I/O	PI5/$\overline{SCK1}$
7	I/O	PC7/RTO7	32	O	PH6	57	I	PF1/AN5	82	I/O	PI4/$\overline{INT1}$
8	I/O	PC6/RTO6	33	O	PH5	58	I	PF0/AN4	83	I/O	PI3/TO
9	I/O	PC5/RTO5	34	O	PH4	59	I	AN3	84	I/O	PI2/$\overline{PWM}$
10	I/O	PC4/RTO4	35	O	PH3	60	I	AN2	85	I/O	PI1/PO
11	I/O	PC3/RTO3	36	O	PH2	61	I	AN1	86	I	PI0/PCK
12	I/O	PC2/PPO18	37	O	PH1	62	I	AN0	87	I	PK0
13	I/O	PC1/PPO17	38	I	PH0	63	I	PG7/EXI1	88	—	GND
14	I/O	PC0/PPO16	39	I	MP	64	I	PG6/EXI0	89	—	V_{DD}
15	I/O	PJ7	40	I/O	$\overline{RST}$	65	I	PG5/SYNC1	90	—	NC
16	I/O	PJ6	41	—	GND	66	I	PG4/SYNC0	91	O	PA7/PPO7
17	I/O	PJ5	42	O	XTAL	67	I	PG3/$\overline{PBCTL}$	92	O	PA6/PPO6
18	I/O	PJ4	43	I	EXTAL	68	I	PG2/DPG	93	O	PA5/PPO5
19	I/O	PJ3	44	I	$\overline{CS0}$	69	I	PG1/DFG	94	O	PA4/PPO4
20	I/O	PJ2	45	I	SI0	70	I	PG0/CFG	95	O	PA3/PPO3
21	I/O	PJ1	46	O	SO0	71	O	PE7/DAB1	96	O	PA2/PPO2
22	I/O	PJ0	47	I/O	$\overline{SCK0}$	72	O	PE6/DAB0	97	O	PA1/PPO1
23	I/O	PD7	48	I/O	PF7/AN11	73	O	PE5/DAA1	98	O	PA0/PPO0
24	I/O	PD6	49	I/O	PF6/AN10	74	O	PE4/DAA0	99	O	PB7/PPO15
25	I/O	PD5	50	I/O	PF5/AN9	75	O	PE3/PWM1	100	O	PB6/PPO14

INPUT

AN0 - AN11	;	A-D CONVERTOR'S ANALOG INPUTS
AV_{REF}	;	A-D CONVERTOR'S REFERENCE VOLTAGE INPUT
CFG	;	CAPSTAN FG INPUT
$\overline{CS0}$	;	SERIAL INTERFACE CHANNLE 0 SELECT INPUT
DPG, DFG	;	DURM PG AND FG INPUTS
$\overline{EC}$	;	EVENT CONTROL INPUT FOR TIMER/COUNTER
EXI0, EXI1	;	FRC CAPTURE UNIT'S EXTERNAL INPUTS
EXTAL	;	CRYSTAL CONNECTION OR EXTERNAL CLOCK INPUTS FOR SYSTEM CLOCK GENERATOR
$\overline{INT0}$ - $\overline{INT2}$	;	INTERRUPT REQUEST INPUTS (FALLING EDGE ACTIVE)
MP	;	MICROPROCESSOR MODE INPUT
$\overline{PBCTL}$	;	PLAYBACK CTL PULSE INPUT
PCK	;	PRESCALER'S EXTERNAL CLOCK INPUT
PE0, PE1	;	INPUTS OF PORT E (PE2 - PE7 ; OUTPUTS)
PF0 - PF3	;	INPUTS OF PORT F (PF4 - PF7 ; OUTPUTS)
PG0 - PG7	;	INPUTS OF PORT G
PI0	;	INPUT OF PORT I (PI1 - PI7 ; INPUTS/OUTPUTS)
PK0	;	INPUT OF PORT K
SI0, SI1	;	SERIAL DATA INPUTS (CHANNLE 0 AND CHANNLE 1)
SYNC0, SYNC1	;	COMPOSITE SYNC SIGNAL INPUTS

OUTPUT

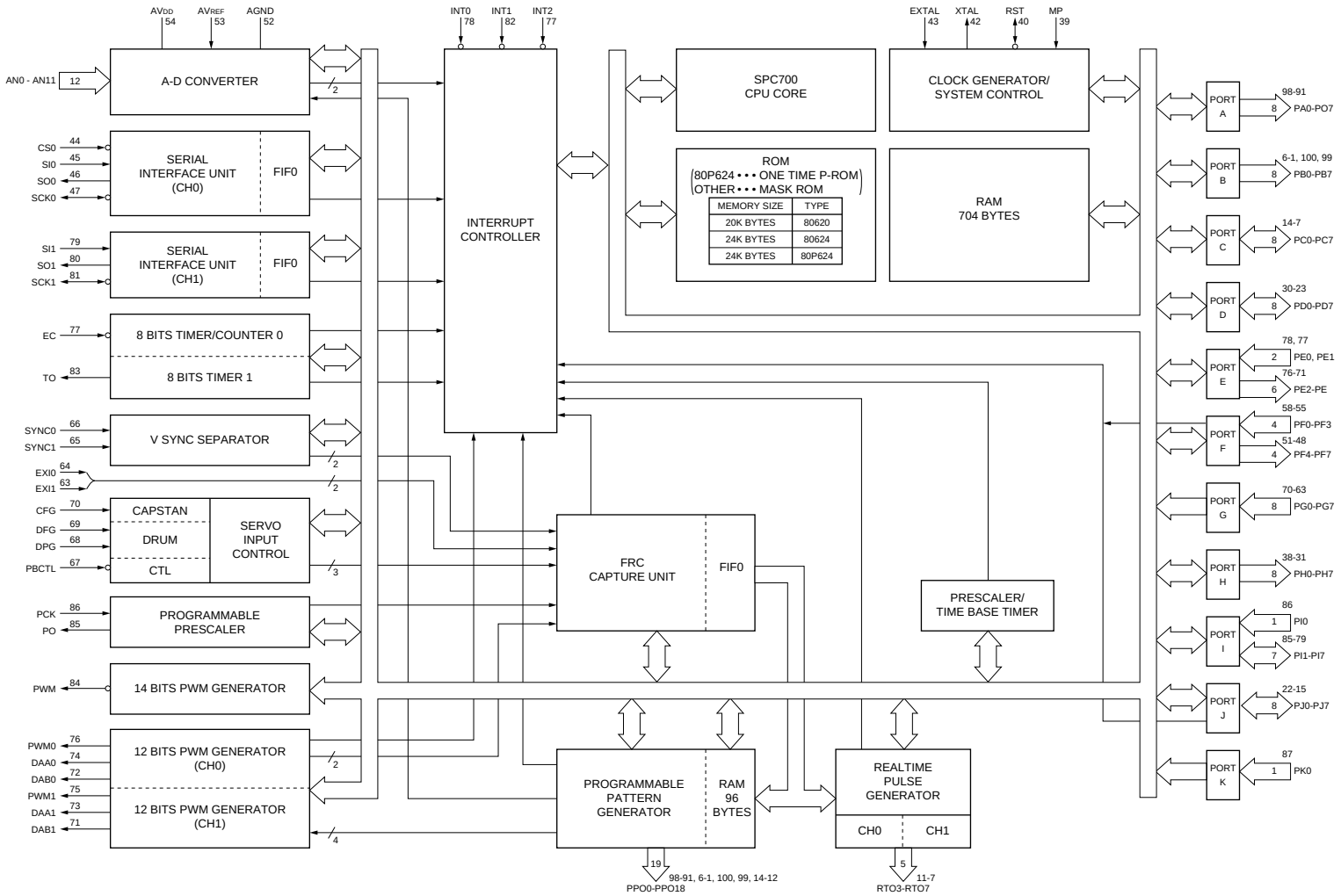
DAA0, DAB0	;	DA GATE PULSE OUTPUTS (12 BITS PWM CHANNLE 0)
DAA1, DAB1	;	DA GATE PULSE OUTPUTS (12 BITS PWM CHANNLE 1)
PA0 - PA7	;	OUTPUTS OF PORT A
PB0 - PB7	;	OUTPUTS OF PORT B
PE2 - PE7	;	OUTPUTS OF PORT E (PE0, PE1 ; INPUTS)
PF4 - PF7	;	OUTPUTS OF PORT F (PF0 - PF3 ; INPUTS)
PH0 - PH7	;	OUTPUTS OF PORT H (N-CH OPEN DRAIN OUTPUTS)
PPO0 - PPO18	;	PROGRAMMABLE PATTERN GENERATOR OUTPUTS
PO	;	PRESCALER OUTPUT
$\overline{PWM}$	;	PULSE WIDTH MODULATION OUTPUT
PWM0, PWM1	;	12 BITS PULSE WIDTH MODULATION OUTPUTS (CHANNLE 0 AND CHANNLE 1)
RTO3 - RTO7	;	REALTIME PULSE GENERATOR OUTPUTS
SO0, SO1	;	SERIAL DATA OUTPUTS (CHANNLE 0 AND CHANNLE 1)
TO	;	TIMER/COUNTER OUTPUT (DUTY 50%)
XTAL	;	CRYSTAL CONNECTION

INPUT/OUTPUT

PC0 - PC7	;	INPUTS/OUTPUTS OF PROT C (BIT PROGRAMMABLE)
PD0 - PD7	;	INPUTS/OUTPUTS OF PROT D (4 BITS PROGRAMMABLE)
PI1 - PI7	;	INPUTS/OUTPUTS OF PROT I (BIT PROGRAMMABLE, PI0 ; INPUT)
PJ0 - PJ7	;	INPUTS/OUTPUTS OF PROT J (BIT PROGRAMMABLE)
$\overline{RST}$	;	SYSTEM RESET INPUT AND POWER ON RESET OUTPUT
$\overline{SCK0}$, $\overline{SCK1}$	;	SERIAL CLOCK INPUTS/OUTPUTS (CHANNLE 0 AND CHANNLE1)

OTHER

AGND	;	A-D CONVERTOR'S GROUND
AV_{DD} (+5V)	;	A-D CONVERTOR'S V_{DD}


AVDD 54
AVREF 53
AGND 52
INT0 78
INT1 82
INT2 77
EXTAL 43
XTAL 42
RST 40
MP 39
AN0 - AN11
12
A-D CONVERTER
2
SERIAL INTERFACE UNIT (CH0)
FIF0
CS0 44
SI0 45
SO0 46
SCK0 47
SERIAL INTERFACE UNIT (CH1)
FIF0
SI1 79
SO1 80
SCK1 81
8 BITS TIMER/COUNTER 0
8 BITS TIMER 1
EC 77
TO 83
V SYNC SEPARATOR
SYNC0 66
SYNC1 65
EXI0 64
EXI1 63
CAPSTAN
DRUM
CTL
SERVO INPUT CONTROL
3
CFG 70
DFG 69
DPG 68
PBCTL 67
PROGRAMMABLE PRESCALER
PCK 86
PO 85
14 BITS PWM GENERATOR
PWM 84
12 BITS PWM GENERATOR (CH0)
12 BITS PWM GENERATOR (CH1)
4
PWM0 76
DAA0 74
DAB0 72
PWM1 75
DAA1 73
DAB1 71
INTERRUPT CONTROLLER
SPC700 CPU CORE
CLOCK GENERATOR/ SYSTEM CONTROL
ROM
(80P624 • • • ONE TIME P-ROM
OTHER • • • MASK ROM)
MEMORY SIZE
TYPE
20K BYTES
80620
24K BYTES
80624
24K BYTES
80P624
RAM 704 BYTES
FRC CAPTURE UNIT
FIF0
PRESCALER/ TIME BASE TIMER
PROGRAMMABLE PATTERN GENERATOR
RAM 96 BYTES
REALTIME PULSE GENERATOR
CH0
CH1
19
98-91, 6-1, 100, 99, 14-12
PPO0-PPO18
5
11-7
RTO3-RTO7
PORT A
8
98-91
PA0-PO7
PORT B
8
6-1, 100, 99
PB0-PB7
PORT C
8
14-7
PC0-PC7
PORT D
8
30-23
PD0-PD7
PORT E
2
78, 77
PE0, PE1
6
76-71
PE2-PE
PORT F
4
58-55
PF0-PF3
4
51-48
PF4-PF7
PORT G
8
70-63
PG0-PG7
PORT H
8
38-31
PH0-PH7
PORT I
1
86
PI0
7
85-79
PI1-PI7
PORT J
8
22-15
PJ0-PJ7
PORT K
1
87
PK0