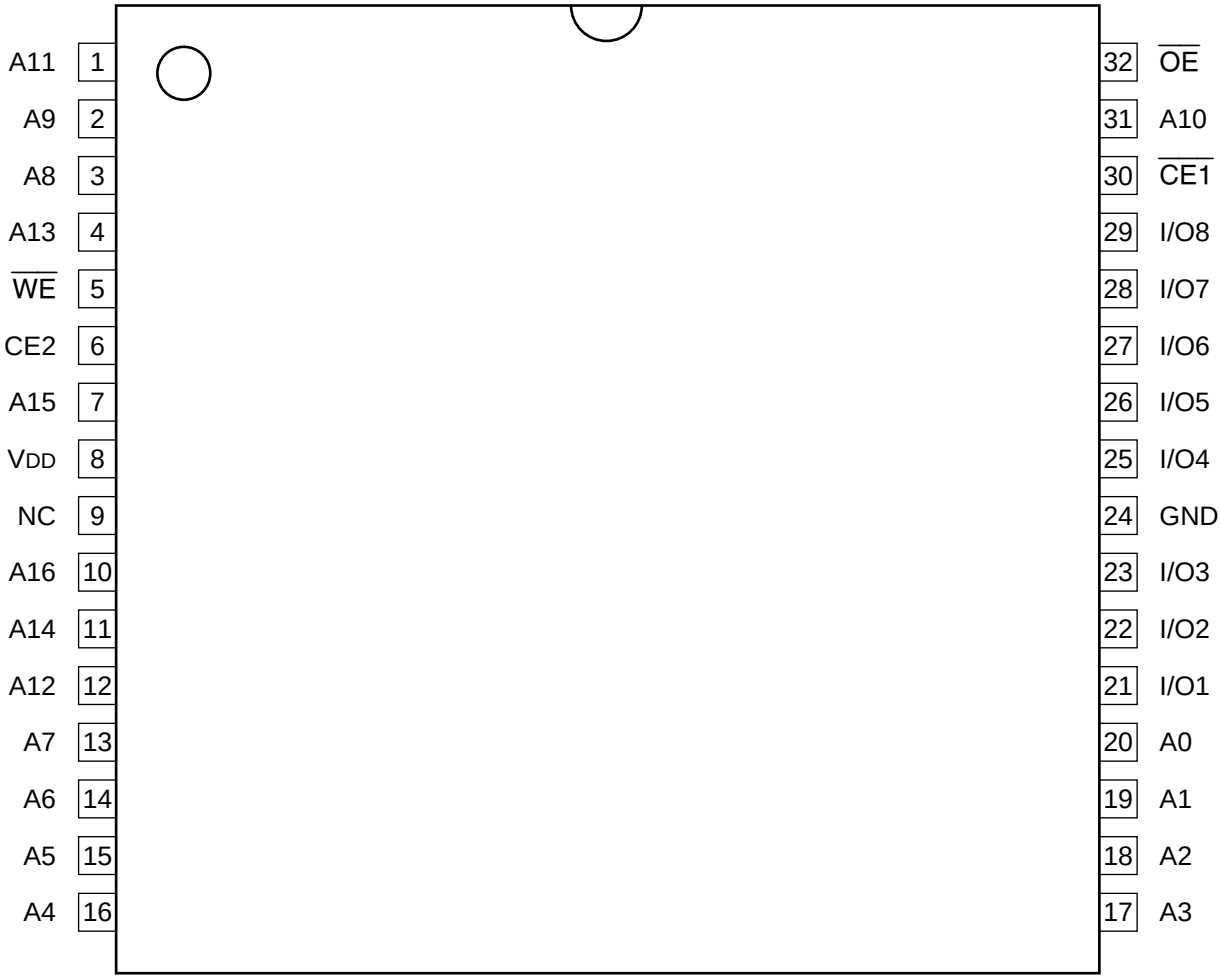
1M (131,072 × 8)-BIT SRAM

—TOP VIEW—

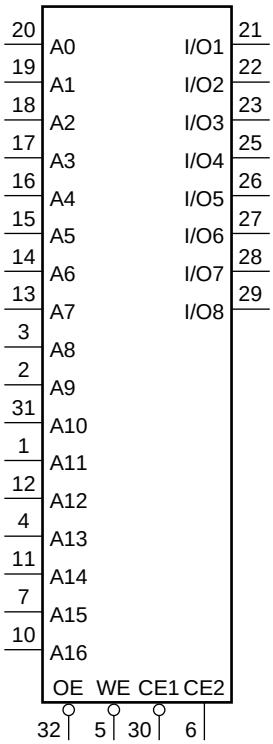


INPUTS

A0 - A16 : ADDRESS
$\overline{CE1}$, CE2 : CHIP ENABLE1, 2
$\overline{WE}$: READ/WRITE ENABLE
$\overline{OE}$: OUTPUT ENABLE

INPUTS/OUTPUTS

I/O1 - I/O8 : DATA



$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I/O TERMINAL
1	×	×	×	NOT SELECT	HIGH IMPEDANCE
×	0	×	×	NOT SELECT	HIGH IMPEDANCE
0	1	1	1	OUTPUT DISABLE	HIGH IMPEDANCE
0	1	0	1	READ	OUTPUT DATA
0	1	×	0	WRITE	INPUT DATA

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE