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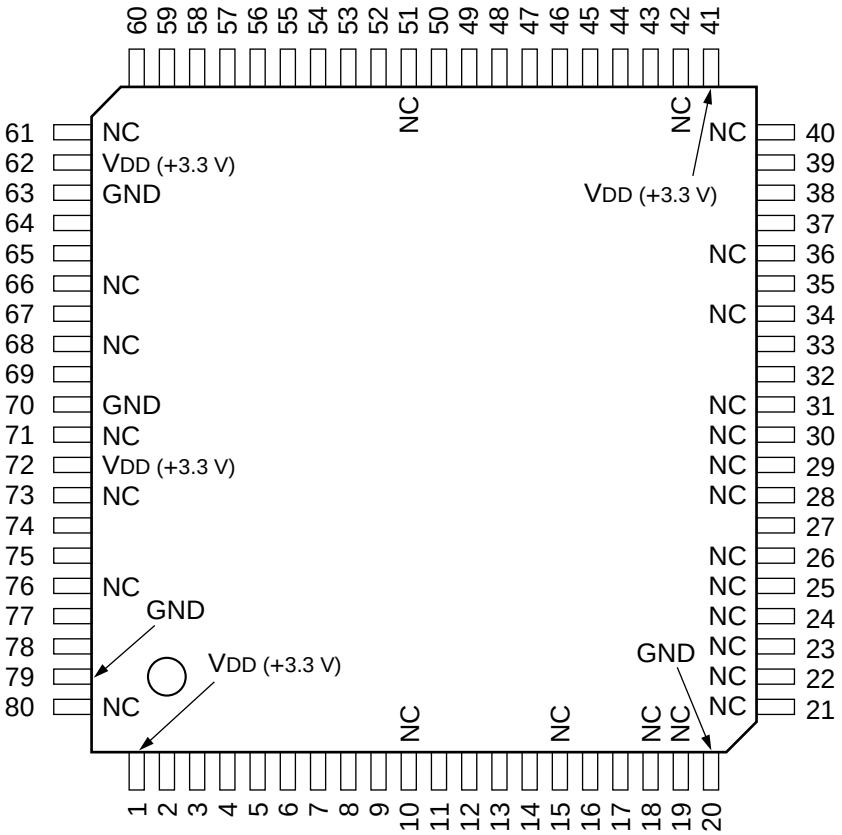
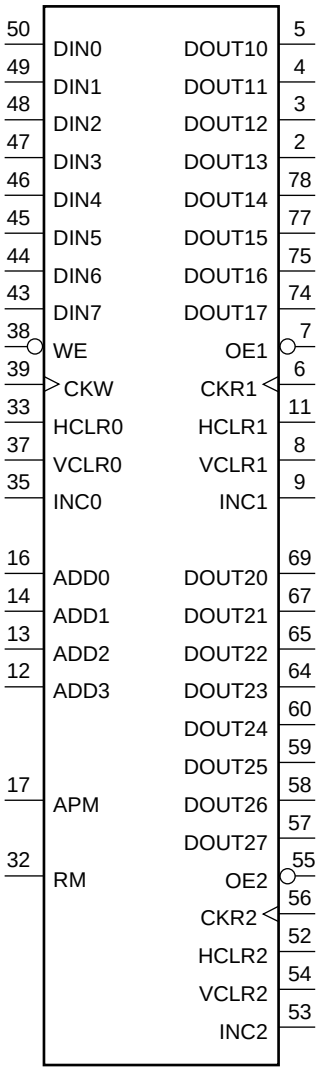
C-MOS 2.4 M (960 × 306 × 8) BITS 3 PORTS VIDEO FIELD MEMORY

—TOP VIEW—





INPUT

ADD0 - ADD3	;	ADDRESS INPUT
APM	;	ADDRESS PRESET MODE ENABLE
CKR1, CKR2	;	PORT 1 OR 2 SHIFT SIGNAL INPUT
CKW	;	PORT 0 SHIFT SIGNAL INPUT
DIN0 - DIN7	;	PORT 0 DATA INPUT
HCLR0 - HCLR2	;	PORT 0 - 2 HORIZONTAL CLEAR
INC0 - INC2	;	PORT 0 - 2 LINE INCREMENT
RM	;	RECURSIVE MODE ENABLE
TE	;	TEST MODE ENABLE
$\overline{\text{VCLR0}}$ - $\overline{\text{VCLR2}}$	;	PORT 0 - 2 VERTICAL CLEAR
$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	;	PORT 1 OR 2 OUTPUT ENABLE
$\overline{\text{WE}}$	;	PORT 0 WRITE ENABLE

OUTPUT

DO10 - DO17	;	PORT 1 DATA OUTPUT
DO20 - DO27	;	PORT 2 DATA OUTPUT

(V_{DD} = +3.3 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{DD}	21	—	NC	41	—	V_{DD}	61	—	NC
2	O	DO13	22	—	NC	42	—	NC	62	—	V_{DD}
3	O	DO12	23	—	NC	43	I	DIN7	63	—	GND
4	O	DO11	24	—	NC	44	I	DIN6	64	O	DO23
5	O	DO10	25	—	NC	45	I	DIN5	65	O	DO22
6	I	CKR1	26	—	NC	46	I	DIN4	66	—	NC
7	I	$\overline{OE1}$	27	—	TE	47	I	DIN3	67	O	DO21
8	I	VCLR1	28	—	NC	48	I	DIN2	68	—	NC
9	I	INC1	29	—	NC	49	I	DIN1	69	O	DO20
10	—	NC	30	—	NC	50	I	DIN0	70	—	GND
11	I	HCLR1	31	—	NC	51	—	NC	71	—	NC
12	I	ADD3	32	I	RM	52	I	HCLR2	72	—	V_{DD}
13	I	ADD2	33	I	HCLR0	53	I	INC2	73	—	NC
14	I	ADD1	34	—	NC	54	I	VCLR2	74	O	DO17
15	—	NC	35	I	INC0	55	I	$\overline{OE2}$	75	O	DO16
16	I	ADD0	36	—	NC	56	I	CKR2	76	—	NC
17	I	APM	37	I	VCLR0	57	O	DO27	77	O	DO15
18	—	NC	38	I	$\overline{WE}$	58	O	DO26	78	O	DO14
19	—	NC	39	I	CKW	59	O	DO25	79	—	GND
20	—	GND	40	—	NC	60	O	DO24	80	—	NC