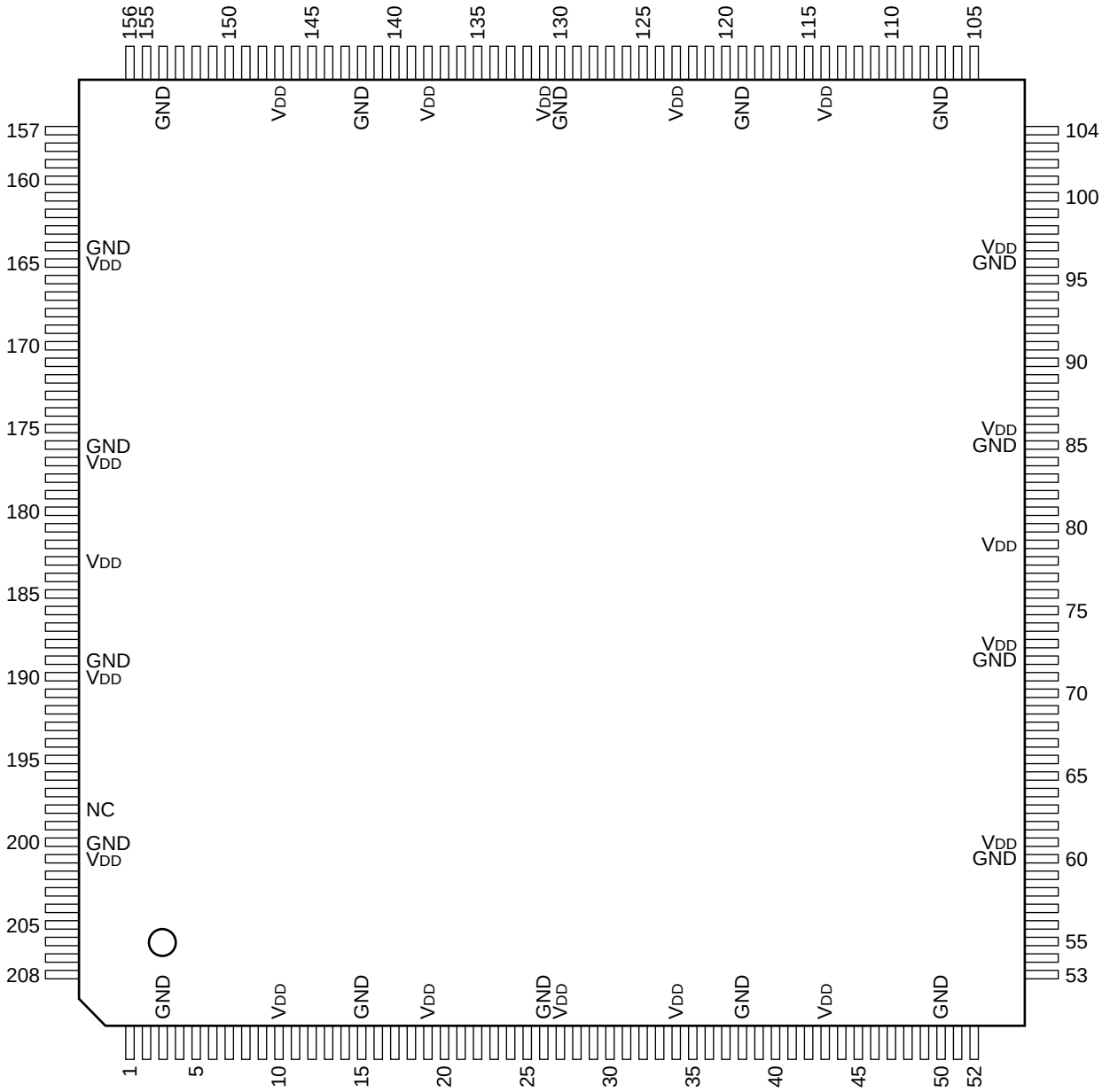
C-MOS FIBER CHANNEL PROTOCOL CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	RX18	53	I	DIP3	105	O	DO30	157	I	A06
2	I	RX17	54	I	DIP2	106	O	DO29	158	I	A05
3	—	GND	55	I	DIP1	107	—	GND	159	I	A04
4	I	RX16	56	I	DIP0	108	O	DO28	160	I	A03
5	I	RX15	57	O	$\overline{\text{DIREQ}}$	109	O	DO27	161	I	A02
6	I	RX14	58	I	$\overline{\text{DIACK}}$	110	O	DO26	162	I	A01
7	I	RX13	59	O	DMACLK	111	O	DO25	163	I	A00
8	I	RX12	60	—	GND	112	O	DO24	164	—	GND
9	I	RX11	61	—	V_{DD}	113	O	DO23	165	—	V_{DD}
10	—	V_{DD}	62	I	DI31	114	—	V_{DD}	166	I/O	D15
11	I	RX10	63	I	DI30	115	O	DO22	167	I/O	D14
12	I	RX09	64	I	DI29	116	O	DO21	168	I/O	D13
13	I	RX08	65	I	DI28	117	O	DO20	169	I/O	D12
14	I	RX07	66	I	DI27	118	O	DO19	170	I/O	D11
15	—	GND	67	I	DI26	119	—	GND	171	I/O	D10
16	I	RX06	68	I	DI25	120	O	DO18	172	I/O	D09
17	I	RX05	69	I	DI24	121	O	DO17	173	I/O	D08
18	I	RX04	70	I	DI23	122	O	DO16	174	I/O	D07
19	—	V_{DD}	71	I	DI22	123	—	V_{DD}	175	I/O	D06
20	I	RX03	72	—	GND	124	O	DO15	176	—	GND
21	I	RX02	73	—	V_{DD}	125	O	DO14	177	—	V_{DD}
22	I	RX01	74	I	DI21	126	O	DO13	178	I/O	D05
23	I	RX00	75	I	DI20	127	O	DO12	179	I/O	D04
24	I	L UNUSE	76	I	DI19	128	O	DO11	180	I/O	D03
25	O	EWRAP	77	I	DI18	129	O	DO10	181	I/O	D02
26	—	GND	78	I	DI17	130	—	GND	182	I/O	D01
27	—	V_{DD}	79	—	V_{DD}	131	—	V_{DD}	183	—	V_{DD}
28	I	TBC	80	I	DI16	132	O	DO09	184	I/O	D00
29	O	TX19	81	I	DI15	133	O	DO08	185	O	$\overline{\text{IRQ}}$
30	O	TX18	82	I	DI14	134	O	DO07	186	I	$\overline{\text{CS}}$
31	O	TX17	83	I	DI13	135	O	DO06	187	I	$\overline{\text{RD}}$
32	O	TX16	84	I	DI12	136	O	DO05	188	I	$\overline{\text{RST}}$
33	O	TX15	85	—	GND	137	O	DO04	189	—	GND
34	—	V_{DD}	86	—	V_{DD}	138	—	V_{DD}	190	—	V_{DD}
35	O	TX14	87	I	DI11	139	O	DO03	191	I	$\overline{\text{WRH}}$
36	O	TX13	88	I	DI10	140	O	DO02	192	I	$\overline{\text{WRL}}$
37	O	TX12	89	I	DI09	141	O	DO01	193	I	SMCK
38	—	GND	90	I	DI08	142	—	GND	194	I	MST
39	O	TX11	91	I	DI07	143	O	DO00	195	I	$\overline{\text{TST}}$
40	O	TX10	92	I	DI06	144	O	DOP3	196	I	$\overline{\text{SM}}$
41	O	TX09	93	I	DI05	145	O	DOP2	197	I	VPD
42	O	TX08	94	I	DI04	146	O	DOP1	198	—	NC
43	—	V_{DD}	95	I	DI03	147	—	V_{DD}	199	I	RBC
44	O	TX07	96	—	GND	148	O	DOP0	200	—	GND
45	O	TX06	97	—	V_{DD}	149	I	A13	201	—	V_{DD}
46	O	TX05	98	I	DI02	150	I	A12	202	O	IDLE
47	O	TX04	99	I	DI01	151	I	A11	203	O	SYNC
48	O	TX03	100	I	DI00	152	I	A10	204	O	TXFRAME
49	O	TX02	101	O	$\overline{\text{DOREQ}}$	153	I	A09	205	O	RXFRAME
50	—	GND	102	I	$\overline{\text{DOACK}}$	154	—	GND	206	O	LCKREF
51	O	TX01	103	I	$\overline{\text{DOE}}$	155	I	A08	207	O	ENCDET
52	O	TX00	104	O	DO31	156	I	A07	208	I	RX19

INPUT

A00 - A13	:	CPU ADDRESS
$\overline{CS}$	:	CHIP SELECT
DI00 - DI31	:	DMA DATA
$\overline{DIACK}$	:	DMA ACKNOWLEDGE
DIP0 - DIP3	:	PARITY BIT
$\overline{DOACK}$	:	DMA ACKNOWLEDGE
$\overline{DOE}$	:	OUTPUT ENABLE
L UNUSE	:	L UNUSE
MST	:	MEMORY SCAN TEST
RBC	:	RECEIVE CLOCK FROM GLM
$\overline{RD}$	:	READ
$\overline{RST}$	:	HARDWARE RESET
RX00 - RX19	:	RECEIVE DATA FROM GLM
$\overline{SM}$	:	SCAN MODE SIGNAL
SMCK	:	SCAN MODE CLOCK
TBC	:	SYSTEM CLOCK
$\overline{TST}$	:	TEST MODE SIGNAL
VPD	:	SCAN MODE SIGNAL
$\overline{WRH}$	:	UPPER BYTE WRITE
$\overline{WRL}$	:	LOWER BYTE WRITE

OUTPUT

ENCDET	:	GLM CONTROL SIGNAL OUTPUT CONTROL
EWRAP	:	GLM CONTROL SIGNAL OUTPUT CONTROL
$\overline{DIREQ}$	:	DMA TRANSFER REQUEST
DMACLK	:	CLOCK OF DMA CONTROL BLOCK
DO00 - DO31	:	DMA DATA
DOP0 - DOP3	:	PARITY BIT
$\overline{DOREQ}$	:	DMA TRANSFER REQUEST
IDLE	:	IDLE STATUS
$\overline{IRQ}$	:	INTERRUPT REQUEST
LCKREF	:	GLM CONTROL SIGNAL OUTPUT CONTROL
RXFRAME	:	FRAME RECEIVE STATUS
SYNC	:	SYNC ACUIRED STATUS
TX00 - TX19	:	TRANSMIT DATA TO GLM
TXFRAME	:	FRAME TRANSMIT STATUS

INPUT/OUTPUT

D00 - D15	:	CPU DATA