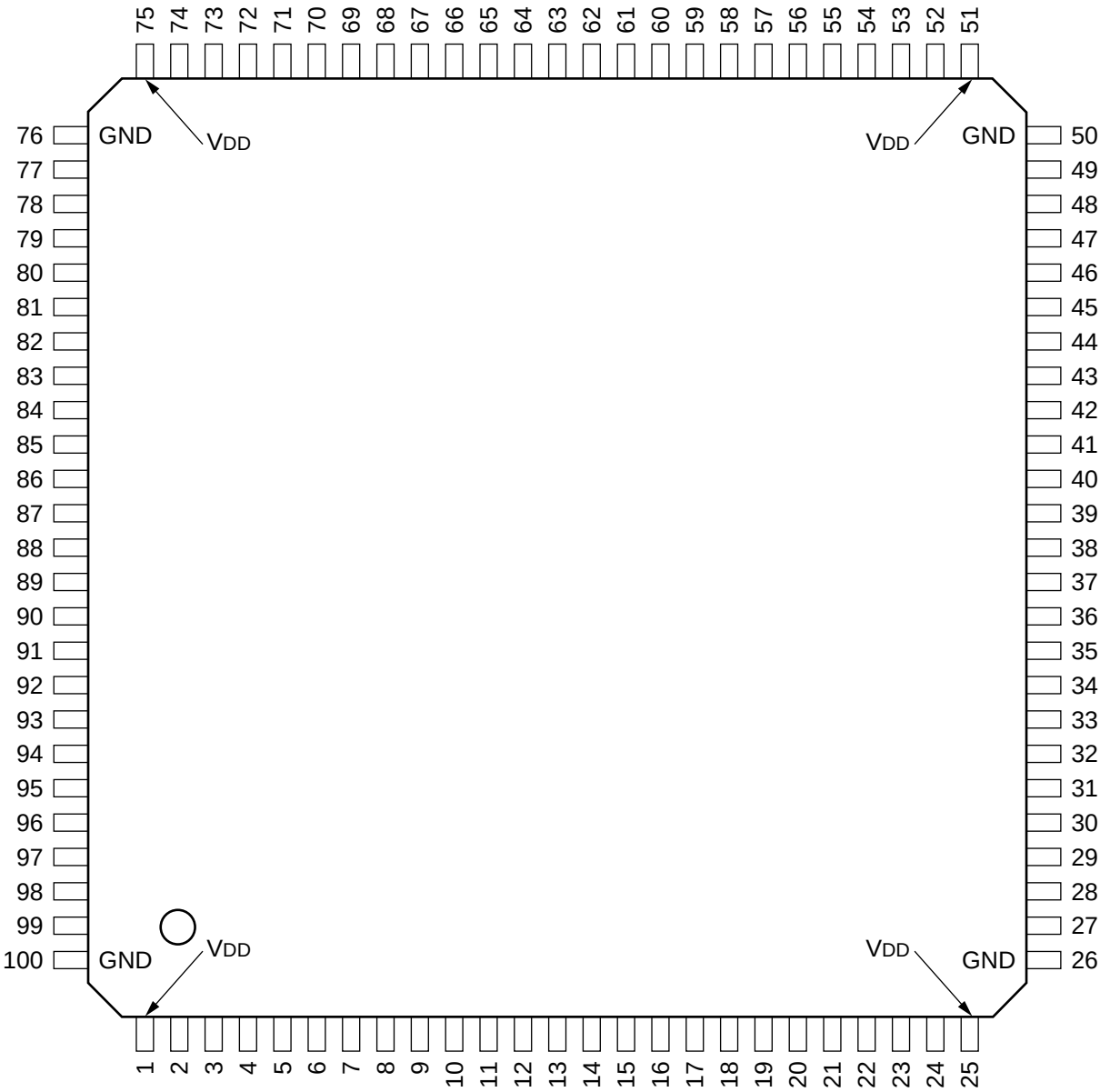
C-MOS VIDEO OUTPUT PROCESSOR (GATE ARRAY)

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{DD}	26	—	GND	51	—	V_{DD}	76	—	GND
2	O	Y4	27	O	U4	52	O	V4	77	O	DIG4
3	O	Y3	28	O	U3	53	O	V3	78	O	DIG3
4	O	Y2	29	O	U2	54	O	V2	79	O	DIG2
5	O	Y1	30	O	U1	55	O	V1	80	O	DIG1
6	O	Y0	31	O	U0	56	O	V0	81	O	DIG0
7	I	IN9	32	—	TSTLC	57	I	XOEV	82	—	TSTD10
8	I	IN8	33	I	XHD	58	I	SMPL	83	—	TSTD9
9	I	IN7	34	—	TSTD00	59	I	XRST	84	—	TSTD8
10	I	IN6	35	I	OE	60	—	TSTA0	85	—	TSTD7
11	I	IN5	36	I	ANCAREA	61	O	SYNC	86	—	TSTD6
12	I	IN4	37	I	XCF	62	I	CK	87	—	TSTD5
13	I	IN3	38	I	CHR	63	—	TSTLR	88	—	TSTD4
14	I	IN2	39	I	EXMASK2	64	I/O	DIO	89	—	TSTD3
15	I	IN1	40	I	EXMASK1	65	—	TSTD15	90	—	TSTD2
16	I	IN0	41	I	ADD	66	—	TSTD14	91	—	TSTD1
17	I	INB1	42	I	XCS	67	—	TSTD13	92	—	TSTA3
18	I	INB2	43	I	CKX	68	—	TSTD12	93	—	TSTA2
19	—	TSTMOD	44	I	CKD	69	—	TSTD11	94	—	TSTA1
20	O	U9	45	O	V9	70	O	DIG9	95	O	Y9
21	O	U8	46	O	V8	71	O	DIG8	96	O	Y8
22	O	U7	47	O	V7	72	O	DIG7	97	O	Y7
23	O	U6	48	O	V6	73	O	DIG6	98	O	Y6
24	O	U5	49	O	V5	74	O	DIG5	99	O	Y5
25	—	V_{DD}	50	—	GND	75	—	V_{DD}	100	—	GND

INPUT

ADD	:	SERIAL INTERFACE ADDRESS
ANCAREA	:	ANCILLARY DATA AREA PULSE
CHR	:	CHARACTER
CK	:	SYSTEM CLOCK
CKD	:	SERIAL INTERFACE CLOCK
CKX	:	SWITCHING TIMING PULSE
EXMASK1, EXMASK2	:	EXTERNAL MASK
IN0 - IN9	:	VIDEO SIGNAL
INB1, INB2	:	EXTENDED VIDEO SIGNAL
OE	:	FIELD ODD/EVEN PULSE
SMPL	:	SAMPLING PULSE
XCF	:	COLOR FRAMING
XCS	:	SERIAL INTERFACE CHIP SELECT
XHD	:	HORIZONTAL DRIVE SIGNAL
XOEV	:	OUTPUT ENABLE
XRST	:	RESET

OUTPUT

DIG0 - DIG9	:	VIDEO DATA
SYNC	:	SYNC PULSE
U0 - U9	:	U SIGNAL
V0 - V9	:	V SIGNAL
Y0 - Y9	:	Y SIGNAL

INPUT/OUTPUT

DIO	:	SERIAL INTERFACE DATA

TEST

TSTA0 - TSTA3	:	TEST
TSTD00	:	TEST
TSTD01 - TSTD15	:	TEST
TSTLC	:	TEST
TSTLR	:	TEST
TSTMOD	:	TEST