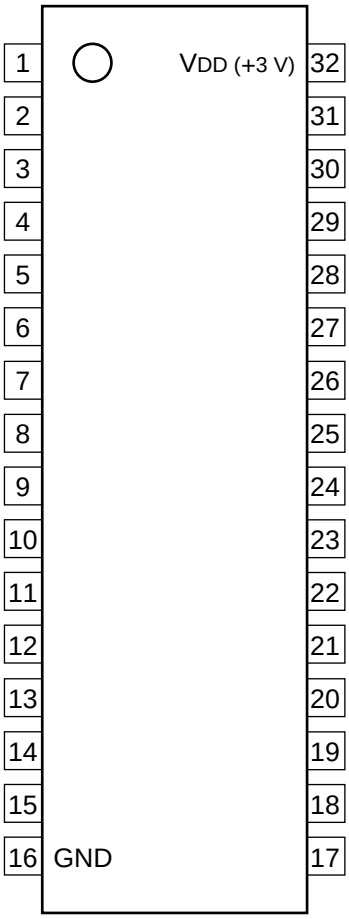
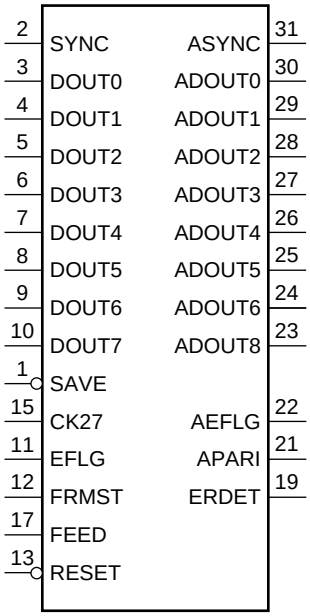
C-MOS INTERVAL ADJUSTER

—TOP VIEW—





(VDD = +3 V)

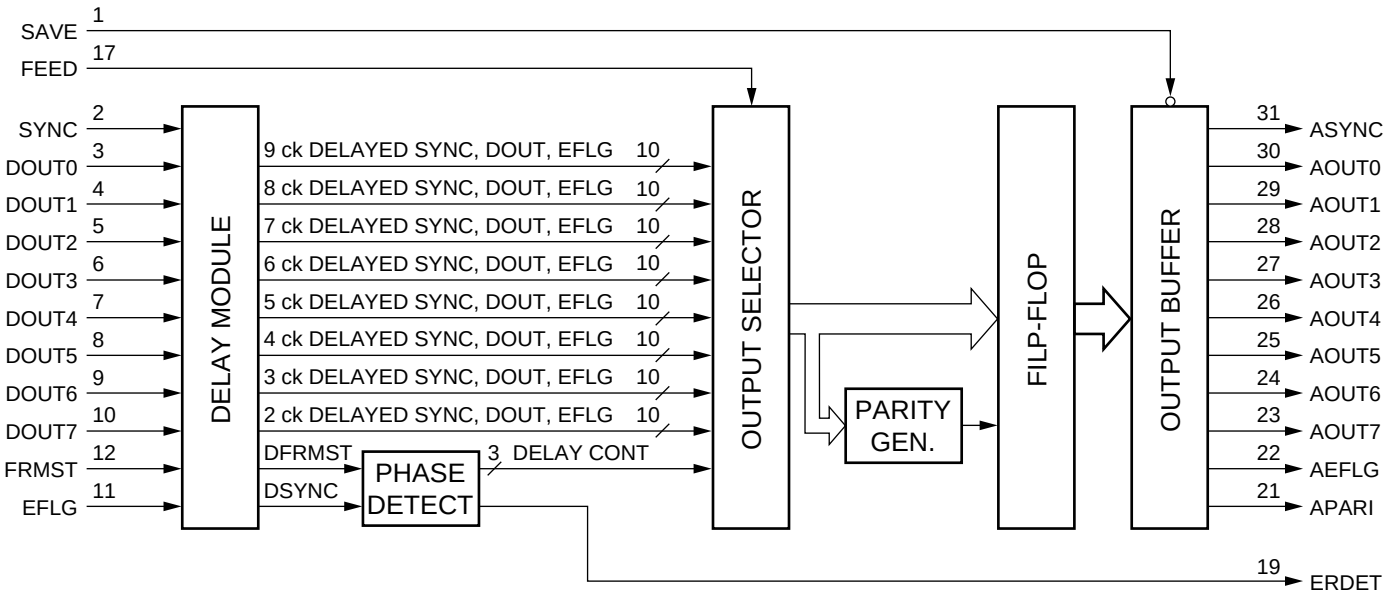
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	SAVE	17	I	FEED
2	I	SYNC	18	—	NC
3	I	DOUT0	19	O	ERDET
4	I	DOUT1	20	—	NC
5	I	DOUT2	21	O	APARI
6	I	DOUT3	22	O	AEFLG
7	I	DOUT4	23	O	ADOUT7
8	I	DOUT5	24	O	ADOUT6
9	I	DOUT6	25	O	ADOUT5
10	I	DOUT7	26	O	ADOUT4
11	I	EFLG	27	O	ADOUT3
12	I	FRMST	28	O	ADOUT2
13	I	RESET	29	O	ADOUT1
14	—	NC	30	O	ADOUT0
15	I	CK27	31	O	ASYNC
16	—	GND	32	—	VDD

INPUT

CK27	:	27 MHz CLOCK
DOUT0 - DOUT7	:	DATA
EFLG	:	EFLG
FEED	:	FEED MODE
FRAMST	:	FRAME START
$\overline{\text{RESET}}$	:	POWER ON RESET
$\overline{\text{SAVE}}$	:	SAVE MODE
SYNC	:	SYNC SIGNAL

OUTPUT

ADOUT0 - ADOUT7	:	ADJUSTED DATA
AEFKG	:	ADJUSTED EFLG
APARI	:	PARITY OF ADJUSTED DATA
ASYNC	:	ADJUSTED SYNC
ERDET	:	PHASE ERROR DETECT


SAVE
1
FEED
17
SYNC
2
DOUT0
3
DOUT1
4
DOUT2
5
DOUT3
6
DOUT4
7
DOUT5
8
DOUT6
9
DOUT7
10
FRMST
12
EFLG
11
DELAY MODULE
9 ck DELAYED SYNC, DOUT, EFLG
10
8 ck DELAYED SYNC, DOUT, EFLG
10
7 ck DELAYED SYNC, DOUT, EFLG
10
6 ck DELAYED SYNC, DOUT, EFLG
10
5 ck DELAYED SYNC, DOUT, EFLG
10
4 ck DELAYED SYNC, DOUT, EFLG
10
3 ck DELAYED SYNC, DOUT, EFLG
10
2 ck DELAYED SYNC, DOUT, EFLG
10
DFRMST
DSYNC
PHASE DETECT
3 DELAY CONT
OUTPUT SELECTOR
PARITY GEN.
FILP-FLOP
OUTPUT BUFFER
31
ASYNC
30
AOUT0
29
AOUT1
28
AOUT2
27
AOUT3
26
AOUT4
25
AOUT5
24
AOUT6
23
AOUT7
22
AEFLG
21
APARI
19
ERDET