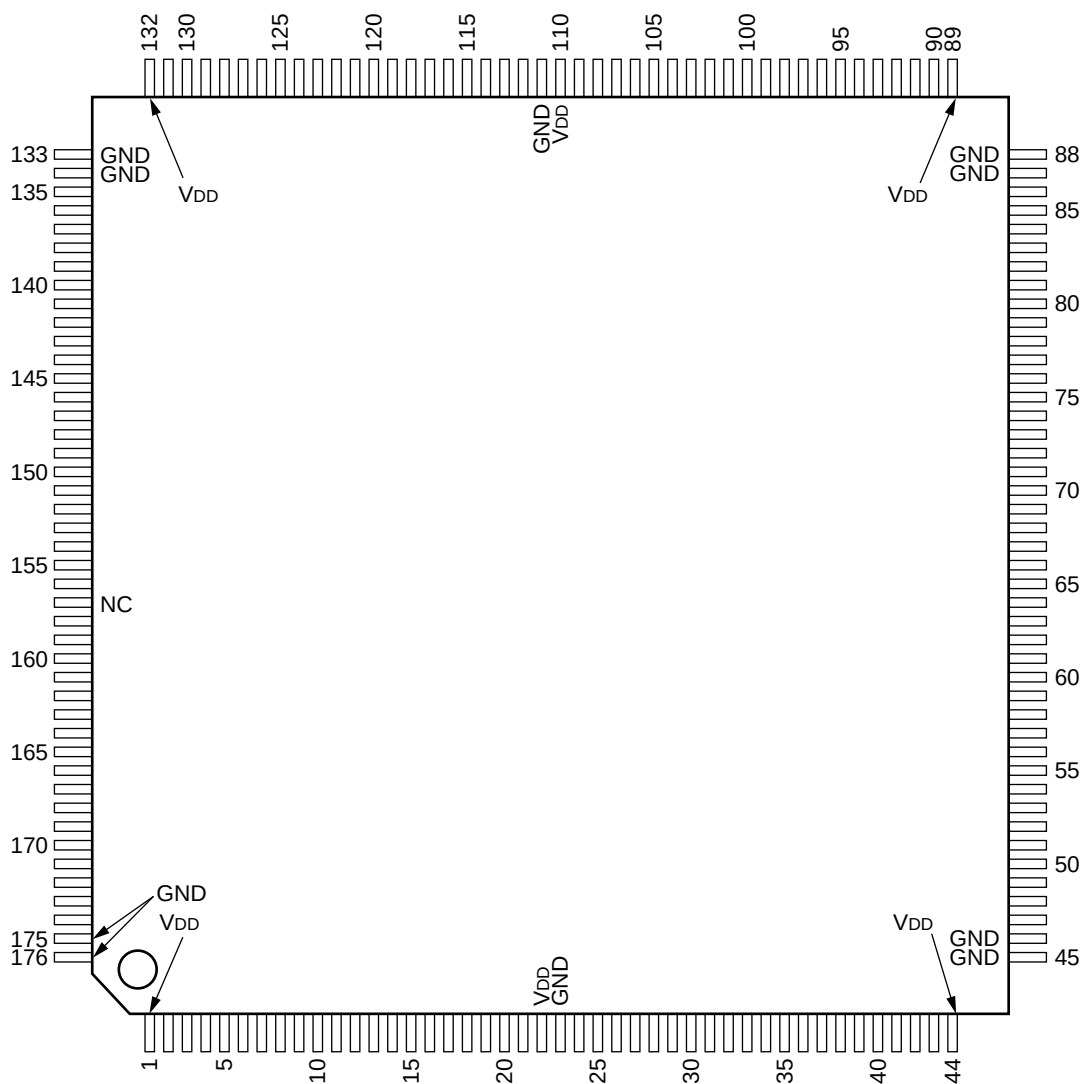


C-MOS CPU R3041 PERIPHERAL

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V _{DD}	45	—	GND	89	—	V _{DD}	133	—	GND
2	O	RDENN	46	—	GND	90	I/O	PIO2P00	134	—	GND
3	O	WRENN	47	I	<u>RESETN</u>	91	I/O	PIO2P01	135	I	INTP0
4	I	CTC1CLK0	48	I	SIOCLK	92	I/O	PIO2P02	136	I	INTP1
5	I	CTC1G0	49	O	SIO1TXD	93	I/O	PIO2P03	137	I	INTP2
6	O	CTC1OUT0	50	I	SIO1RXD	94	I/O	PIO2P04	138	I	INTP3
7	I	CTC1CLK1	51	O	SIO1INT	95	I/O	PIO2P05	139	I	INTP4
8	I	CTC1G1	52	I	<u>SIO2CTS</u>	96	I/O	PIO2P06	140	I	INTP5
9	O	CTC1OUT1	53	I	<u>SIO2DSR</u>	97	I/O	PIO2P07	141	I	INTP6
10	I	CTC1CLK2	54	O	SIO2TXD	98	I	TEST2	142	I	INTP7
11	I	CTC1G2	55	I	SIO2RXD	99	I/O	PIO2P10	143	O	INT
12	O	CTC1OUT2	56	O	SIO2INT	100	I/O	PIO2P11	144	I/O	SIO2BRK
13	O	EXTDENN	57	O	SIORDN	101	I/O	PIO2P12	145	I	EXTFRAME
14	O	IOENN	58	O	SIOWRN	102	I/O	PIO2P13	146	O	FRAME
15	I	<u>BEN0</u>	59	O	SIOCDN	103	I/O	PIO2P14	147	O	VINT
16	I	<u>BEN1</u>	60	O	SIOBAN	104	I/O	PIO2P15	148	O	S8W4CSN
17	I	<u>BEN2</u>	61	I/O	PIO1P00	105	I/O	PIO2P16	149	I	SYSCLKN
18	I	<u>BEN3</u>	62	I/O	PIO1P01	106	I/O	PIO2P17	150	I	<u>DATAENN</u>
19	I	A0	63	I/O	PIO1P02	107	I	TEST3	151	I	<u>BURSTN</u>
20	I	A1	64	I/O	PIO1P03	108	I/O	PIO2P20	152	I	<u>LASTN</u>
21	I	A23	65	I/O	PIO1P04	109	I/O	PIO2P21	153	I	<u>RDN</u>
22	—	V _{DD}	66	I/O	PIO1P05	110	—	V _{DD}	154	I	<u>WRN</u>
23	—	GND	67	I/O	PIO1P06	111	—	GND	155	O	ACKN
24	I	A24	68	I/O	PIO1P07	112	I/O	PIO2P22	156	O	RDCENN
25	I	A25	69	I	TEST0	113	I/O	PIO2P23	157	—	NC
26	I	A26	70	I/O	PIO1P10	114	I/O	PIO2P24	158	O	S8W3CSN1
27	I	A27	71	I/O	PIO1P11	115	I/O	PIO2P25	159	O	S8W3CSN2
28	I	A28	72	I/O	PIO1P12	116	I/O	PIO2P26	160	O	S8W3CSN3
29	I/O	D0	73	I/O	PIO1P13	117	I/O	PIO2P27	161	O	S8W3CSN4
30	I/O	D1	74	I/O	PIO1P14	118	O	S16W2CSN	162	O	S8W3CSN5
31	I/O	D2	75	I/O	PIO1P15	119	O	S16W3CSN	163	O	S8W3CSN6
32	I/O	D3	76	I/O	PIO1P16	120	I	CTC2CLK0	164	O	V8W3CSN
33	I/O	D4	77	I/O	PIO1P17	121	I	CTC2G0	165	O	FIFOREN1
34	I/O	D5	78	I	TEST1	122	O	CTC2OUT0	166	O	FIFOREN2
35	I/O	D6	79	I/O	PIO1P20	123	I	CTC2CLK1	167	O	FIFOREN3
36	I/O	D7	80	I/O	PIO1P21	124	I	CTC2G1	168	O	FIFOREN4
37	O	FLASHCSN	81	I/O	PIO1P22	125	O	CTC2OUT1	169	O	FIFOWEN1
38	O	SRAM1CS	82	I/O	PIO1P23	126	I	CTC2CLK2	170	O	FIFOWEN2
39	O	SRAM2CS	83	I/O	PIO1P24	127	I	CTC2G2	171	O	FIFOWEN3
40	O	WRENNNA	84	I/O	PIO1P25	128	O	CTC2OUT2	172	O	FIFOWEN4
41	O	WRENNB	85	I/O	PIO1P26	129	O	HALFCLK	173	O	FIFORCKN
42	O	WRENNC	86	I/O	PIO1P27	130	O	V8W6CSN	174	O	IOENN2
43	O	WRENNND	87	—	GND	131	I	<u>VARWAITN</u>	175	—	GND
44	—	V _{DD}	88	—	GND	132	—	V _{DD}	176	—	GND

INPUT

A0, A1 ; ADDRESS BUS
 A23 - A28 ; ADDRESS BUS
 $\overline{\text{BEN0}} - \overline{\text{BEN3}}$; 1st TO 4th BYTE SELECT
 BURSTN ; CPU BURST
 CTC1CLK0 - CTC1CLK2 ; CTC CLOCK
 CTC1G0 - CTC1G2 ; CTC GATE
 CTC2CLK0 - CTC2CLK2 ; CTC2 CLOCK
 CTC2G0 - CTC2G2 ; CTC2 GATE
 $\overline{\text{DATAENN}}$; CPU DATA ENABLE
 EXTFRAME ; EXTERNAL FRAME
 INTP0 - INTP7 ; INTERRUPT
 LASTN ; CPU LAST
 RDN ; CPU READ
 RESETN ; CPU RESET
 SIO1RXD ; SIO1 RECEIVE DATA
 SIO2CTS ; SIO2 CTS
 SIO2DSR ; SIO2 DSR
 SIO2RXD ; SIO2 RECEIVE DATA
 SIOCLK ; SIO CLOCK
 SYSCLKN ; CPU SYSTEM CLOCK
 TEST0 - TEST3 ; TEST
 VARWAITN ; VARIABLE WAIT
 WRN ; CPU WRITE

OUTPUT

ACKN ; CPU ACKNOWLEDGE
 CTC1OUT0 - CTC1OUT2 ; CTC1 OUT
 CTC2OUT0 - CTC2OUT2 ; CTC2 OUT
 EXTDENN ; READ/WRITE SELECT
 FIFORCKN ; FIFO READ CLOCK
 FIFOREN1 - FIFOREN4 ; FIFO READ ENABLE
 FIFOWEN1 - FIFOWEN4 ; FIFO WRITE ENABLE
 FLASHCSN ; FLASH ROM CHIP SELECT
 FRAME ; FRAME
 HALFCLK ; DIVIDED-BY-TWO SYSTEM CLOCK
 INT ; INTERRUPT
 IOENN ; DATA BUS DRIVER ENABLE
 IOENN2 ; 2nd DATA BUS DRIVER ENABLE
 RDCENN ; CPU READ CHIP ENABLE
 RDENN ; READ
 S16W2CSN ; 16-BIT 2-WAIT CHIP ENABLE
 S16W3CSN ; 16-BIT 3-WAIT CHIP ENABLE
 S8W3CSN1 - S8W3CSN6 ; 8-BIT 3-WAIT CHIP ENABLE
 S8W4CSN ; 8-BIT 4-WAIT CHIP ENABLE
 SIO1INT ; SIO1 INTERRUPT
 SIO1TXD ; SIO1 TRANSMIT DATA
 SIO2INT ; SIO2 INTERRUPT
 SIO2TXD ; SIO2 TRANSMIT DATA
 SIOBAN ; SIO B/A
 SIOCDN ; SIO C/D
 SIORDN ; SIO READ
 SIOWRN ; SIO WRITE
 SRAM1CS ; SRAM1 CHIP SELECT
 SRAM2CS ; SRAM2 CHIP SELECT
 V8W3CSN ; VARIABLE WAIT 8-BIT 3-WAIT CHIP ENABLE
 V8W6CSN ; VARIABLE WAIT 8-BIT 6-WAIT CHIP ENABLE
 VINT ; FRAME INTERRUPT
 WRENN ; WRITE
 WRENN A - WRENN D ; SRAM 1st TO 4th BYTE WRITE

INPUT/OUTPUT

D0 - D7 ; DATA BUS
 PIO1P00 - PIO1P07 ; PIO1 PORT0
 PIO1P10 - PIO1P17 ; PIO1 PORT1
 PIO1P20 - PIO1P27 ; PIO1 PORT2
 PIO2P00 - PIO2P07 ; PIO2 PORT0
 PIO2P10 - PIO2P17 ; PIO2 PORT1
 PIO2P20 - PIO2P27 ; PIO2 PORT2
 SIO2BRK ; SIO2 SYNC/BRK

