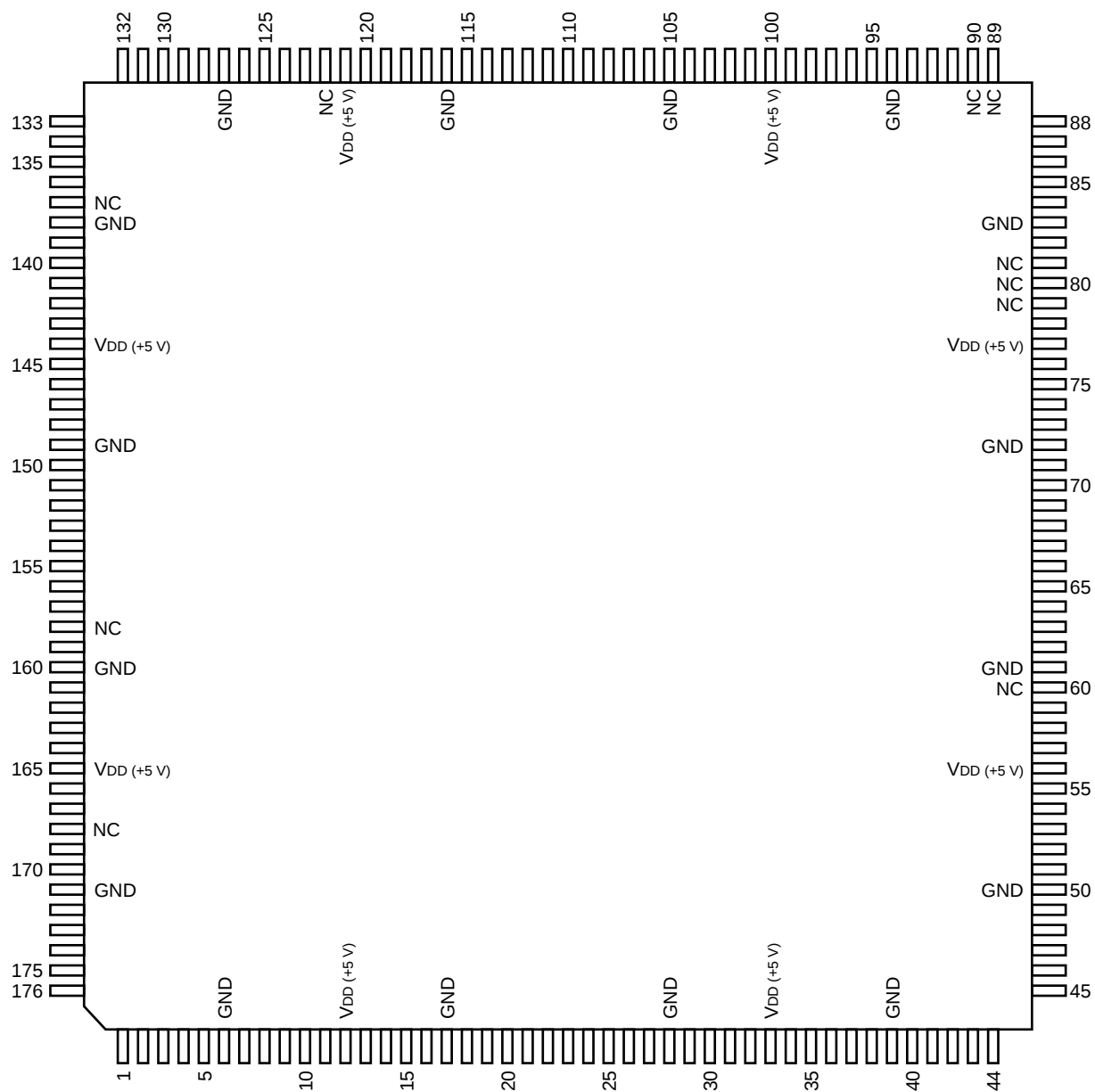


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## C-MOS A/V DATA PB PROCESS (GATE ARRAY)

- TOP VIEW -



(VDD = +5 V)

| PIN No. | I/O | SIGNAL        | PIN No. | I/O | SIGNAL     | PIN No. | I/O | SIGNAL      | PIN No. | I/O | SIGNAL         |
|---------|-----|---------------|---------|-----|------------|---------|-----|-------------|---------|-----|----------------|
| 1       | O   | RFADR5        | 45      | O   | INT_OUT    | 89      | —   | NC          | 133     | I   | SYSA5          |
| 2       | O   | RFADR6        | 46      | O   | TCWEN      | 90      | —   | NC          | 134     | I   | SYSA6          |
| 3       | O   | RFADR7        | 47      | O   | TCWRSTN    | 91      | O   | WSYSEN      | 135     | I   | SYSA7          |
| 4       | O   | TABLE_A_EN    | 48      | O   | VEND       | 92      | I   | EXT_SPC_FDO | 136     | I   | SYSA8          |
| 5       | O   | TABLE_B_EN    | 49      | O   | VSYNC      | 93      | O   | SPC_FDO     | 137     | —   | NC             |
| 6       | —   | GND           | 50      | —   | GND        | 94      | —   | GND         | 138     | —   | GND            |
| 7       | O   | OE1           | 51      | O   | DOUT0      | 95      | O   | WFADR0      | 139     | I   | CLK            |
| 8       | O   | OE2           | 52      | O   | DOUT1      | 96      | O   | WFADR1      | 140     | O   | TEST1          |
| 9       | O   | OE3           | 53      | O   | DOUT2      | 97      | O   | WFADR2      | 141     | O   | TEST2          |
| 10      | O   | OE4           | 54      | O   | DOUT3      | 98      | O   | WFADR3      | 142     | O   | TEST3          |
| 11      | O   | OE5           | 55      | O   | DOUT4      | 99      | O   | WFADR4      | 143     | O   | TEST4          |
| 12      | —   | VDD           | 56      | —   | VDD        | 100     | —   | VDD         | 144     | —   | VDD            |
| 13      | O   | OE6           | 57      | O   | DOUT5      | 101     | O   | WFADR5      | 145     | O   | TEST5          |
| 14      | O   | OE7           | 58      | O   | DOUT6      | 102     | O   | WFADR6      | 146     | O   | TEST6          |
| 15      | O   | READLOPLS     | 59      | O   | DOUT7      | 103     | O   | WFADR7      | 147     | O   | TEST7          |
| 16      | O   | READRSTART    | 60      | —   | NC         | 104     | O   | MWRST       | 148     | O   | TEST8          |
| 17      | —   | GND           | 61      | —   | GND        | 105     | —   | GND         | 149     | —   | GND            |
| 18      | O   | RE1           | 62      | O   | VWE        | 106     | O   | GPI1        | 150     | I   | DATA0          |
| 19      | I   | RCB_L4        | 63      | O   | VWRST      | 107     | O   | GPI2        | 151     | I   | DATA1          |
| 20      | I   | RCB_RE1       | 64      | O   | VRE        | 108     | I/O | SYSD0       | 152     | I   | DATA2          |
| 21      | I   | RCB_AGOP_ST   | 65      | O   | VRRST      | 109     | I/O | SYSD1       | 153     | I   | DATA3          |
| 22      | I   | RCB_VGOP_ST   | 66      | O   | FIFOEN     | 110     | I/O | SYSD2       | 154     | I   | DATA4          |
| 23      | I   | TEST_DC       | 67      | O   | AWE        | 111     | I/O | SYSD3       | 155     | I   | DATA5          |
| 24      | I   | TEST_RCB      | 68      | O   | AWRST      | 112     | I/O | SYSD4       | 156     | I   | DATA6          |
| 25      | I   | RCB_N_GOP_GET | 69      | O   | ARE        | 113     | I/O | SYSD5       | 157     | I   | DATA7          |
| 26      | I   | RCB_E_OF_V_S  | 70      | O   | ARRST      | 114     | I/O | SYSD6       | 158     | —   | NC             |
| 27      | I   | RCB_RSYSPEN   | 71      | O   | FIFORS     | 115     | I/O | SYSD7       | 159     | O   | APEN           |
| 28      | —   | GND           | 72      | —   | GND        | 116     | —   | GND         | 160     | —   | GND            |
| 29      | I   | HD            | 73      | O   | CMDRRSTN   | 117     | O   | GPI3        | 161     | O   | REVOUT         |
| 30      | I   | FP            | 74      | I   | ADEN1      | 118     | O   | GPI4        | 162     | I   | MB2_RSYSPEN    |
| 31      | O   | REFH          | 75      | I   | ADEN2      | 119     | O   | GPI5        | 163     | I   | MB2_NEXT_GET   |
| 32      | O   | REFF          | 76      | I   | WSCFULL_IN | 120     | O   | GPI6        | 164     | I   | MB2_END_SECTOR |
| 33      | —   | VDD           | 77      | —   | VDD        | 121     | —   | VDD         | 165     | —   | VDD            |
| 34      | O   | OE8           | 78      | I   | TEST_MODE  | 122     | —   | NC          | 166     | I   | AUDIO_CORE_WE  |
| 35      | O   | RECFULL       | 79      | —   | NC         | 123     | I   | RICCS       | 167     | I   | TEST_MODE2     |
| 36      | O   | WSCFULL       | 80      | —   | NC         | 124     | I   | SYSRD       | 168     | —   | NC             |
| 37      | O   | WSTART        | 81      | —   | NC         | 125     | I   | SYSWR       | 169     | I   | EXT_RE         |
| 38      | O   | READ_GATE     | 82      | O   | TX_GATE    | 126     | I   | SYSRST      | 170     | O   | MRRST          |
| 39      | —   | GND           | 83      | —   | GND        | 127     | —   | GND         | 171     | —   | GND            |
| 40      | O   | ASYNC         | 84      | O   | BUF01REN1  | 128     | I   | SYSA0       | 172     | O   | RFADR0         |
| 41      | O   | AEND          | 85      | O   | BUF01OE    | 129     | I   | SYSA1       | 173     | O   | RFADR1         |
| 42      | I   | INT0          | 86      | O   | BUF02REN1  | 130     | I   | SYSA2       | 174     | O   | RFADR2         |
| 43      | I   | INT1          | 87      | O   | BUF02OE    | 131     | I   | SYSA3       | 175     | O   | RFADR3         |
| 44      | I   | INT2          | 88      | O   | BUF01EF    | 132     | I   | SYSA4       | 176     | O   | RFADR4         |

**INPUT**

|                             |                                       |
|-----------------------------|---------------------------------------|
| <u>ADEN1</u> , <u>ADEN2</u> | ; SDDI APPLICATION DATA ENABLE 1, 2   |
| <u>AUDIO_CORE_WE</u>        | ; AUDIO CORE WRITE ENABLE             |
| <u>CLK</u>                  | ; SYSTEM CLOCK                        |
| <u>DATA0 - DATA7</u>        | ; DATA IN 0 - 7                       |
| <u>EXT_RE</u>               | ; EXTERNAL READ ENABLE                |
| <u>EXT_SPC_FDO</u>          | ; TEST PIN                            |
| <u>FP</u>                   | ; REFERENCE FRAME                     |
| <u>HD</u>                   | ; REFERENCE H                         |
| <u>INT0 - INT2</u>          | ; SDDI INT 0 - 2                      |
| <u>MB2_END_SECTOR</u>       | ; END OF VIDEO SECTOR PULSE IN        |
| <u>MB2_NEXT_GET</u>         | ; NEXT GOP GET START PULSE IN         |
| <u>MB2_RSYSPEN</u>          | ; READ SYSTEM PRE ENABLE IN           |
| <u>RCB_AGOP_ST</u>          | ; READ CONTROL AUDIO GOP START        |
| <u>RCB_E_OF_V_S</u>         | ; READ CONTROL END OF VIDEO SECTOR    |
| <u>RCB_L4</u>               | ; READ CONTROL LENGTH 4               |
| <u>RCB_N_GOP_GET</u>        | ; READ CONTROL NEXT GOP GET PULSE     |
| <u>RCB_RE1</u>              | ; READ CONTROL READ ENABLE 1          |
| <u>RCB_RSYSPEN</u>          | ; READ CONTROL READ SYSTEM PRE ENABLE |
| <u>RCB_VGOP_ST</u>          | ; READ CONTROL VIDEO GOP START        |
| <u>RICCS</u>                | ; CXD8991R CHIP SELECT                |
| <u>SYSA0 - SYSA8</u>        | ; CPU ADDRESS 0 - 8                   |
| <u>SYSRST</u>               | ; SYSTEM RESET                        |
| <u>SYSRD</u>                | ; CXD8991R READ ENABLE                |
| <u>SYSWR</u>                | ; CXD8991R WRITE ENABLE               |
| <u>TEST_DC</u>              | ; TEST PIN                            |
| <u>TEST_MODE</u>            | ; TEST PIN                            |
| <u>TEST_MODE2</u>           | ; TEST PIN                            |
| <u>TEST_RCB</u>             | ; TEST PIN                            |
| <u>WSCFULL_IN</u>           | ; WRITE SECTOR FULL IN                |

**INPUT/OUTPUT**

|                      |                      |
|----------------------|----------------------|
| <u>SYSD0 - SYSD7</u> | ; CPU DATA BUS 0 - 7 |
|----------------------|----------------------|

**OUTPUT**

|                                       |                                      |
|---------------------------------------|--------------------------------------|
| <u>AEND</u>                           | ; AUDIO END PULSE                    |
| <u>APEN</u>                           | ; AUDIO PROCESS ENABLE               |
| <u>ARE</u>                            | ; AUDIO CORE READ ENABLE             |
| <u>ARRST</u>                          | ; AUDIO CORE READ RESET              |
| <u>ASYNC</u>                          | ; AUDIO SYNC BIT                     |
| <u>AWE</u>                            | ; AUDIO CORE WRITE ENABLE            |
| <u>AWRST</u>                          | ; AUDIO CORE WRITE RESET             |
| <u>BUF01EF</u>                        | ; SPC I/F* : BUFFER 1 EMPTY FLAG     |
| <u>BUF01OE</u> , <u>BUF02OE</u>       | ; SPC I/F* : BUFFER 1, 2 OUT ENABLE  |
| <u>BUF01REN1</u> , <u>BUF02REN1</u>   | ; SPC I/F* : BUFFER 1, 2 READ ENABLE |
| <u>CMDRRSTN</u>                       | ; COMMAND FIFO READ RESET            |
| <u>DOUT0 - DOUT7</u>                  | ; DATA OUT 0 - 7                     |
| <u>FIFOEN</u>                         | ; FIFO POWER ON ENABLE               |
| <u>FIFORS</u>                         | ; FIFO POWER ON RESET                |
| <u>GPI1 - GPI6</u>                    | ; GPI PORT 1 - 6                     |
| <u>INT_OUT</u>                        | ; INTERRUPT TO CPU                   |
| <u>MRRST</u>                          | ; MAIN MEMORY READ RESET             |
| <u>MWRST</u>                          | ; MAIN MEMORY WRITE RESET            |
| <u>OE1 - OE8</u>                      | ; MAIN MEMORY OUTPUT ENABLE 1 - 8    |
| <u>RE1</u>                            | ; MAIN MEMORY READ ENABLE 1          |
| <u>READ_GATE</u>                      | ; MAIN MEMORY READ GATE              |
| <u>READLOPLS</u>                      | ; READ ADDRESS LOAD PULSE            |
| <u>READRSTART</u>                     | ; READ ADDRESS START PULSE           |
| <u>RECFULL</u>                        | ; READ SECTOR FULL PULSE             |
| <u>REFF</u>                           | ; REFERENCE FRAME                    |
| <u>REFH</u>                           | ; REFERENCE H                        |
| <u>REVOUT</u>                         | ; MAIN MEMORY VIDEO READ ENABLE      |
| <u>RFADR0 - RFADR7</u>                | ; MAIN MEMORY READ ADDRESS 0 - 7     |
| <u>SPC_FDO</u>                        | ; MAIN MEMORY WRITE ENABLE           |
| <u>TABLE_A_EN</u> , <u>TABLE_B_EN</u> | ; TABLE A, B ENABLE                  |
| <u>TCWEN</u>                          | ; MESSAGE FIFO WRITE ENABLE          |
| <u>TCWRSTN</u>                        | ; MESSAGE FIFO WRITE RESET           |
| <u>TEST1 - TEST8</u>                  | ; TEST PIN 1 - 8                     |
| <u>TX_GATE</u>                        | ; SDDI CORE IC ENABLE                |
| <u>VEND</u>                           | ; VIDEO END PULSE                    |
| <u>VRE</u>                            | ; VIDEO CORE READ ENABLE             |
| <u>VRRST</u>                          | ; VIDEO CORE READ RESET              |
| <u>VSYNC</u>                          | ; VIDEO SYNC BIT                     |
| <u>VWE</u>                            | ; VIDEO CORE WRITE ENABLE            |
| <u>VWRST</u>                          | ; VIDEO CORE WRITE RESET             |
| <u>WFADR0 - WFADR7</u>                | ; MAIN MEMORY WRITE ADDRESS 0 - 7    |
| <u>WSCFULL</u>                        | ; WRITE SECTOR FULL PULSE            |
| <u>WSTART</u>                         | ; WRITE START PULSE                  |
| <u>WSYSEN</u>                         | ; WRITE SYSTEM ENABLE                |

\* SPC I/F : SCSI PROTOCOL CONTROLLER INTERFACE