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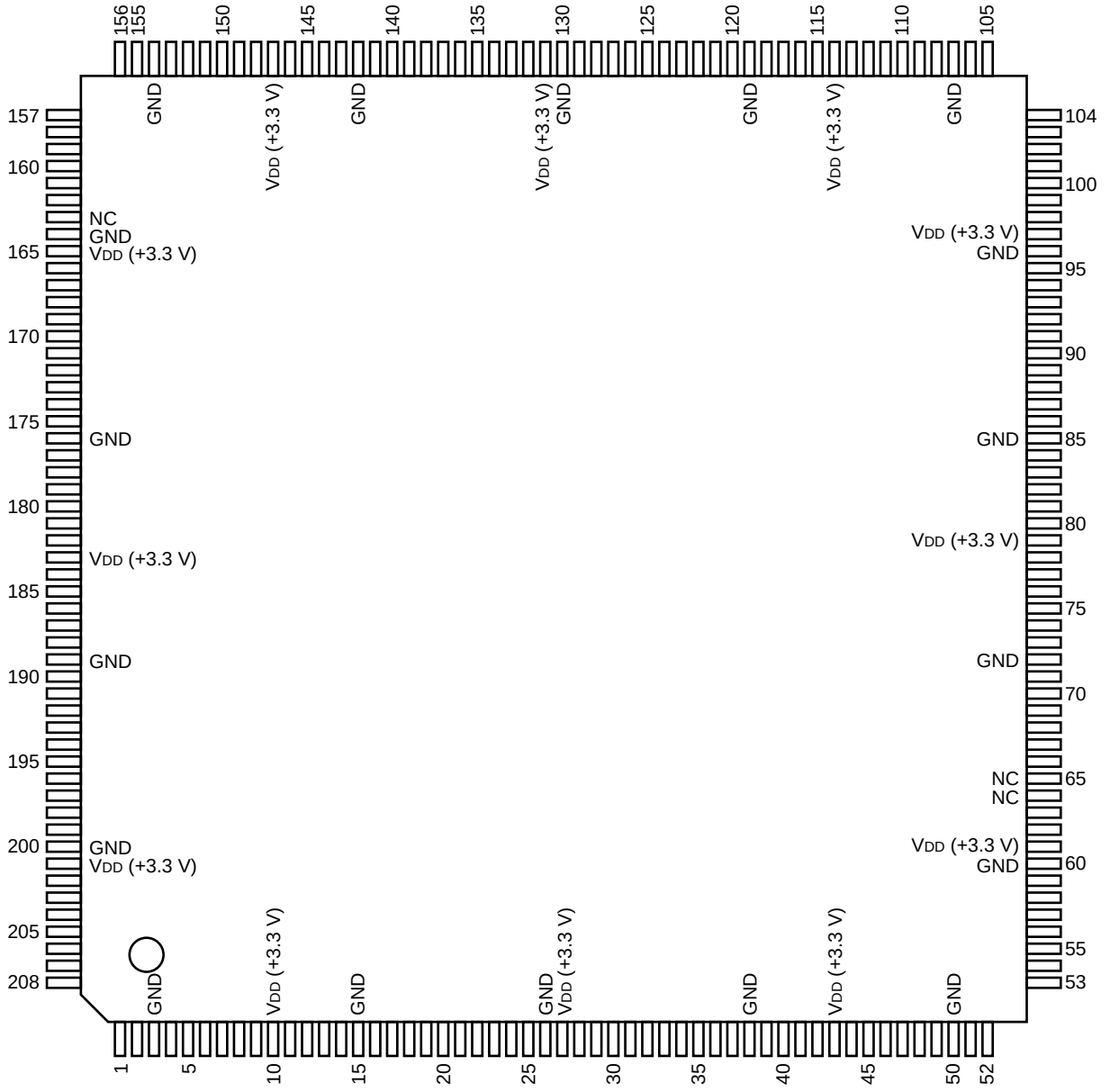
IL11

C-MOS SDDI PACKING (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +3.3 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	$\overline{\text{OVDWE7}}$	43	—	V_{DD}	85	—	GND	127	I	IBRR78	169	O	$\overline{\text{OVRE6}}$
2	O	$\overline{\text{OVDWE6}}$	44	I	ISXIGOPT	86	O	OCRPRTY	128	I	IFS128	170	O	$\overline{\text{OVRE5}}$
3	—	GND	45	I	ISXIFRM	87	O	$\overline{\text{OCRSYNC}}$	129	I	IFS1	171	O	$\overline{\text{OVRE4}}$
4	O	$\overline{\text{OVDWE5}}$	46	I	ISXIH	88	O	OCRDT7	130	—	GND	172	O	$\overline{\text{OVRE3}}$
5	O	$\overline{\text{OVDWE4}}$	47	I	$\overline{\text{IG2RSTN}}$	89	O	OCRDT6	131	—	V_{DD}	173	O	$\overline{\text{OVRE2}}$
6	O	$\overline{\text{OVDWE3}}$	48	I	IREFFRM	90	O	OCRDT5	132	O	OAPFWRP	174	O	$\overline{\text{OVRE1}}$
7	O	$\overline{\text{OVDWE2}}$	49	I	IREFH	91	O	OCRDT4	133	O	OAPFWD8	175	O	$\overline{\text{OVRE0}}$
8	O	$\overline{\text{OVDWE1}}$	50	—	GND	92	O	OCRDT3	134	O	OAPFWD7	176	—	GND
9	O	$\overline{\text{OVDWE0}}$	51	I	$\overline{\text{ISXSYNC}}$	93	O	OCRDT2	135	O	OAPFWD6	177	O	$\overline{\text{OVRSTR}}$
10	—	V_{DD}	52	I	ISXDT7	94	O	OCRDT1	136	O	OAPFWD5	178	O	$\overline{\text{OVOEN74}}$
11	O	$\overline{\text{OVDRW}}$	53	I	ISXDT6	95	O	OCRDT0	137	O	OAPFWD4	179	O	$\overline{\text{OVOEN30}}$
12	O	OWREMK	54	I	ISXDT5	96	—	GND	138	O	OAPFWD3	180	O	$\overline{\text{OARSTR}}$
13	O	$\overline{\text{OWRSYNC}}$	55	I	ISXDT4	97	—	V_{DD}	139	O	OAPFWD2	181	O	$\overline{\text{OARE1}}$
14	O	OWRVDPR	56	I	ISXDT3	98	O	$\overline{\text{OATEND}}$	140	O	OAPFWD1	182	O	$\overline{\text{OARE0}}$
15	—	GND	57	I	ISXDT2	99	O	$\overline{\text{OVEND}}$	141	O	OAPFWD0	183	—	V_{DD}
16	O	$\overline{\text{OATRWN}}$	58	I	ISXDT1	100	O	$\overline{\text{OAEND}}$	142	—	GND	184	I	$\overline{\text{XACK}}$
17	O	$\overline{\text{OATWEN}}$	59	I	ISXDT0	101	I	$\overline{\text{IATINT}}$	143	O	$\overline{\text{OADRW}}$	185	I/O	BCK
18	I/O	BSYBUS7	60	—	GND	102	I	$\overline{\text{IVINT}}$	144	O	$\overline{\text{OADWE0}}$	186	I	$\overline{\text{XTCK}}$
19	I/O	BSYBUS6	61	—	V_{DD}	103	I	$\overline{\text{IAINT}}$	145	O	$\overline{\text{OADWE1}}$	187	I	IRDEMK
20	I/O	BSYBUS5	62	I	ISXPRTY	104	I	$\overline{\text{IATEN}}$	146	O	$\overline{\text{OAWEALL}}$	188	I	IRDPRTY
21	I/O	BSYBUS4	63	I	IVWCK	105	I	$\overline{\text{IVEN}}$	147	—	V_{DD}	189	—	GND
22	I/O	BSYBUS3	64	—	NC	106	I	$\overline{\text{IAEN}}$	148	O	$\overline{\text{OAACT}}$	190	I	IRDDT7
23	I/O	BSYBUS2	65	—	NC	107	—	GND	149	O	OASPIN	191	I	IRDDT6
24	I/O	BSYBUS1	66	I	$\overline{\text{IVGOPST}}$	108	O	ODLFS2	150	O	OSPLAT	192	I	IRDDT5
25	I/O	BSYBUS0	67	I	IAREFF	109	O	ODLFS1	151	O	OGT5F	193	I	IRDDT4
26	—	GND	68	O	OVPFW2GT	110	O	OPKI12	152	I	$\overline{\text{IAUDSIML}}$	194	I	IRDDT3
27	—	V_{DD}	69	O	OAPWGT	111	O	OPKI34	153	I	IA5FSQ2	195	I	IRDDT2
28	I	IDIRRDH	70	O	OPFR2GT	112	O	OPKI56	154	—	GND	196	I	IRDDT1
29	I	$\overline{\text{IPKCSN}}$	71	O	OPFRAGT	113	O	OPKI78	155	I	IA5FSQ1	197	I	IRDDT0
30	I	$\overline{\text{ISTRBN}}$	72	—	GND	114	—	V_{DD}	156	I	IA5FSQ0	198	I	$\overline{\text{IRDSYNC}}$
31	I	ISTAT1	73	I	$\overline{\text{XTRE}}$	115	I	IPKO12	157	O	OVANCLN	199	O	OWRDT7
32	I	ISTAT0	74	I	$\overline{\text{XTWE}}$	116	I	IPKO34	158	O	OVIDXLN	200	—	GND
33	I/O	BMON7	75	I	$\overline{\text{XMM}}$	117	I	IPKO56	159	O	$\overline{\text{OAATOEN}}$	201	—	V_{DD}
34	I/O	BMON6	76	O	ORDPERR	118	I	IPKO78	160	I	IPKO12B	202	O	OWRDT6
35	I/O	BMON5	77	O	OCOREF	119	—	GND	161	I	IPKO34B	203	O	OWRDT5
36	I/O	BMON4	78	O	OCOREH	120	I	IBYP12	162	I	IVAGCK	204	O	OWRDT4
37	I/O	BMON3	79	—	V_{DD}	121	I	IBYP34	163	—	NC	205	O	OWRDT3
38	—	GND	80	I	$\overline{\text{XSM}}$	122	I	IBYP56	164	—	GND	206	O	OWRDT2
39	I/O	BMON2	81	I	$\overline{\text{XTST}}$	123	I	IBYP78	165	—	V_{DD}	207	O	OWRDT1
40	I/O	BMON1	82	I	IVASELF	124	I	IBRR12	166	O	$\overline{\text{OATRSTRN}}$	208	O	OWRDT0
41	I/O	BMON0	83	I	IVASELH	125	I	IBRR34	167	O	$\overline{\text{OATREN}}$			
42	O	OSXRFRM	84	I	IVRCK	126	I	IBRR56	168	O	$\overline{\text{OVRE7}}$			

INPUT

IA5FSQ0 - IA5FSQ2 ; AUDIO 5F SEQUENCE 0 - 2
$\overline{\text{IAEN}}$; AUDIO ENABLE PULSE
$\overline{\text{IAINT}}$; AUDIO INTERRUPT PULSE
IAREFF ; AUDIO REFERENCE FRAME
$\overline{\text{IATEN}}$; ATTRIBUTE ENABLE PULSE
$\overline{\text{IATINT}}$; ATTRIBUTE INTERRUPT PULSE
IAUDSIML ; AUDIO SIMULATION MODE
IBRR12 ; AUDIO BRR DATA IN 1/2-CH
IBRR34 ; AUDIO BRR DATA IN 3/4-CH
IBRR56 ; AUDIO BRR DATA IN 5/6-CH
IBRR78 ; AUDIO BRR DATA IN 7/8-CH
IBYP12 ; AUDIO NON-BRR DATA IN 1/2-CH
IBYP34 ; AUDIO NON-BRR DATA IN 3/4-CH
IBYP56 ; AUDIO NON-BRR DATA IN 5/6-CH
IBYP78 ; AUDIO NON-BRR DATA IN 7/8-CH
IDIRRDH ; SYSTEM INTERFACE DIRECTION
IFS1 ; AUDIO FS1
IFS128 ; AUDIO FS128
$\overline{\text{IG2RSTN}}$; 2 × GOP RESET
$\overline{\text{IPKCSN}}$; SYSTEM INTERFACE CHIP SELECT
IPKO12 ; AUDIO PACKED DATA IN 1/2-CH
IPKO34 ; AUDIO PACKED DATA IN 3/4-CH
IPKO56 ; AUDIO PACKED DATA IN 5/6-CH
IPKO78 ; AUDIO PACKED DATA IN 7/8-CH
IPKO12B ; AUDIO PACKED DATA - B 1/2-CH
IPKO34B ; AUDIO PACKED DATA - B 3/4-CH
IRDDT0 - IRDDT7 ; FIFO READ DATA 0 - 7
IRDEMK ; FIFO READ END MARK
$\overline{\text{IRDPRTY}}$; FIFO READ PARITY
$\overline{\text{IRDSYNC}}$; FIFO READ SYNC
IREFFRM ; FRAME PULSE (REF. LOCK)
IREFH ; H PULSE (REF. LOCK)
ISTAT0, ISTAT1 ; SYSTEM INTERFACE ADDRESS 0, 1
$\overline{\text{ISTRBN}}$; SYSTEM INTERFACE STROBE
ISXDT0 - ISXDT7 ; ENC OUTPUT DATA 0 - 7
ISXIFRM ; FRAME PULSE (INPUT LOCK)
ISXIGOPT ; GOP START PULSE
ISXIH ; H PULSE (INPUT LOCK)
$\overline{\text{ISXPRTY}}$; ENC OUTPUT PARITY
$\overline{\text{ISXSYNC}}$; ENC OUTPUT SYNC
IVAGCK ; VANC GEN. 27 MHz CLOCK
IVASELF ; VANC SELECTED FRAME
IVASELH ; VANC SELECTED H
$\overline{\text{IVEN}}$; VIDEO ENABLE PULSE
$\overline{\text{IVGOPST}}$; VIDEO GOP START
$\overline{\text{IVINT}}$; VIDEO INTERRUPT PULSE
IVRCK ; READ 27 MHz CLOCK
IVWCK ; VIDEO WRITE 27 MHz CLOCK
$\overline{\text{XACK}}$, $\overline{\text{XMM}}$, $\overline{\text{XSM}}$
$\overline{\text{XTCK}}$, $\overline{\text{XTRE}}$ } ; IC TEST
$\overline{\text{XTST}}$, $\overline{\text{XTWE}}$

OUTPUT

OAACT	; AUDIO ACTIVE PULSE
OAATOEN	; AUDIO/ATTRIBUTE FIFO OUTPUT ENABLE
OADRW	; AUDIO FIFO RESET WRITE
OADWE0, OADWE1	; AUDIO FIFO WRITE ENABLE 0, 1
OAEND	; AUDIO END PULSE
OAPFWD0 - OAPFWD8	; AUDIO FIFO WRITE DATA 0 - 8
OAPFWPR	; AUDIO FIFO WRITE PARITY
OAPWGT	; AUDIO WRITE GOP
OARE0, OARE1	; AUDIO FIFO READ ENABLE 0, 1
OARSTR	; AUDIO FIFO RESET READ
OASPIN	; AUDIO S/P INPUT DATA
OATEND	; ATTRIBUTE END PULSE
OATREN	; ATTRIBUTE FIFO READ ENABLE
OATRSTRN	; ATTRIBUTE FIFO RESET READ
OATRWN	; ATTRIBUTE FIFO RESET WRITE
OATWEN	; ATTRIBUTE FIFO WRITE ENABLE
OAWEALL	; AUDIO FIFO WRITE ENABLE ALL
OCOREF	; SDDI CORE FRAME
OCOREH	; SDDI CORE H
OCRDT0 - OCRDT7	; PACKED DATA 0 - 7
OCRPRTY	; PACKED DATA PARITY
OCRSYNC	; PACKED DATA SYNC
ODLFS1, ODLFS2	; DELAYED FS1, 2
OGT5F	; AUDIO 5F PULSE
OPFR2GT	; READ 2 × GOP
OPFRAGT	; ADVANCE READ GOP
OPKI12	; AUDIO PACK DATA OUT 1/2-CH
OPKI34	; AUDIO PACK DATA OUT 3/4-CH
OPKI56	; AUDIO PACK DATA OUT 5/6-CH
OPKI78	; AUDIO PACK DATA OUT 7/8-CH
ORDPERR	; READ PARITY ERROR
OSPLAT	; AUDIO S/P LATCH PULSE
OSXRFRM	; ENC READ START
OVANCLN	; VANC LINE PULSE
OVDRW	; VIDEO FIFO RESET WRITE
OVDWE0 - OVDWE7	; VIDEO FIFO WRITE ENABLE 0 - 7
OVEND	; VIDEO END PULSE
OVIDXLN	; VIDEO INDEX LINE PULSE
OVOEN30	; VIDEO FIFO OUTPUT ENABLE 3 - 0
OVOEN74	; VIDEO FIFO OUTPUT ENABLE 7 - 4
OVPFW2GT	; VIDEO WRITE 2 × GOP
OVRE0 - OVRE7	; VIDEO FIFO READ ENABLE 0 - 7
OVRSTR	; VIDEO FIFO RESET READ
OWRDT0 - OWRDT7	; VIDEO FIFO WRITE DATA 0 - 7
OWREMK	; VIDEO FIFO WRITE END PULSE
OWRSYNC	; VIDEO FIFO WRITE SYNC
OWRVDPR	; VIDEO FIFO WRITE PARITY

INPUT/OUTPUT

BCK	; IC TEST
BMON0 - BMON7	; MONITOR OUTPUT 0 - 7
BSYBUS0 - BSYBUS7	; SYSTEM INTERFACE BUS 0 - 7