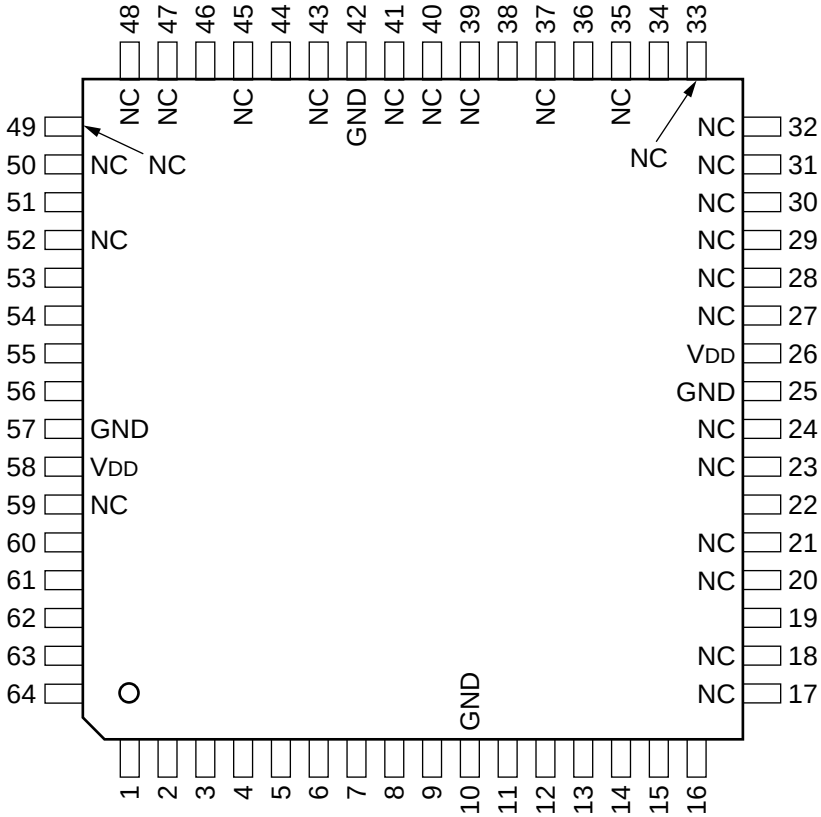
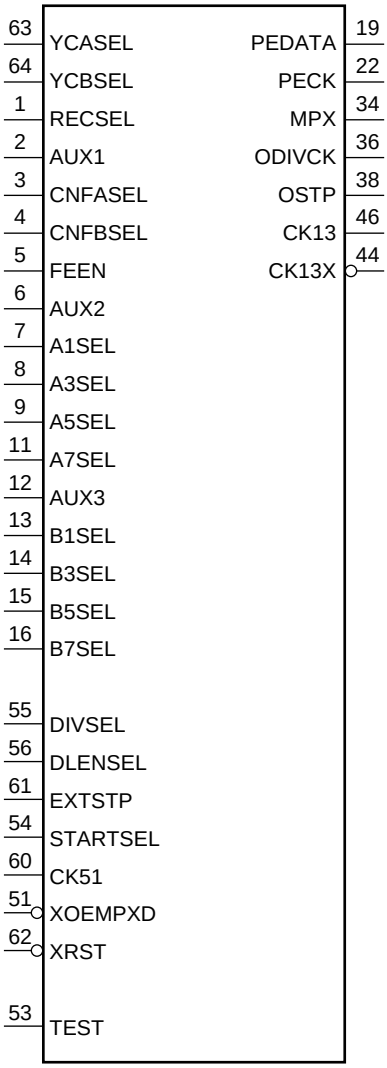
# C-MOS DIGITAL MULTIPLEX ENCODER

—TOP VIEW—



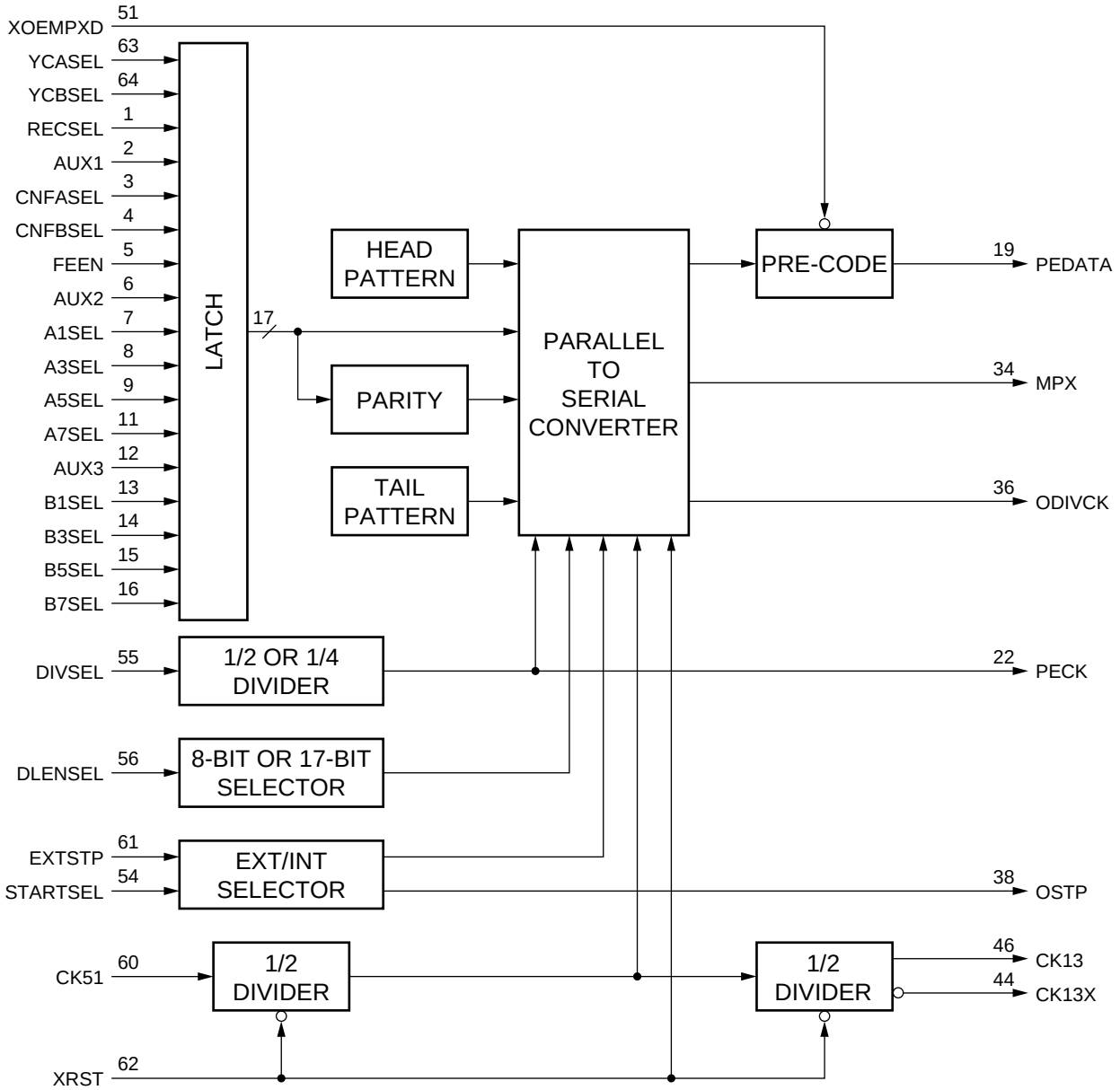
| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | I | RECSEL | 17 | — | NC | 33 | — | NC | 49 | — | NC |
| 2 | I | AUX1 | 18 | — | NC | 34 | O | MPX | 50 | — | NC |
| 3 | I | CNFASEL | 19 | O | PEDATA | 35 | — | NC | 51 | I | $\overline{\text{XOEMPXD}}$ |
| 4 | I | CNFBSEL | 20 | — | NC | 36 | O | ODIVCK | 52 | — | NC |
| 5 | I | FEEN | 21 | — | NC | 37 | — | NC | 53 | I | TEST |
| 6 | I | AUX2 | 22 | O | PECK | 38 | O | OSTP | 54 | I | STARTSEL |
| 7 | I | A1SEL | 23 | — | NC | 39 | — | NC | 55 | I | DIVSEL |
| 8 | I | A3SEL | 24 | — | NC | 40 | — | NC | 56 | I | DLENSEL |
| 9 | I | A5SEL | 25 | — | GND | 41 | — | NC | 57 | — | GND |
| 10 | — | GND | 26 | — | $V_{DD}$ | 42 | — | GND | 58 | — | $V_{DD}$ |
| 11 | I | A7SEL | 27 | — | NC | 43 | — | NC | 59 | — | NC |
| 12 | I | AUX3 | 28 | — | NC | 44 | O | $\overline{\text{CK13X}}$ | 60 | I | CK51 |
| 13 | I | B1SEL | 29 | — | NC | 45 | — | NC | 61 | I | EXTSTP |
| 14 | I | B3SEL | 30 | — | NC | 46 | O | CK13 | 62 | I | $\overline{\text{XRST}}$ |
| 15 | I | B5SEL | 31 | — | NC | 47 | — | NC | 63 | I | YCASEL |
| 16 | I | B7SEL | 32 | — | NC | 48 | — | NC | 64 | I | YCBSEL |

**INPUT**

A1SEL ; A1/A2 PB HEAD SELECT
A3SEL ; A3/A4 PB HEAD SELECT
A5SEL ; A5/A6 PB HEAD SELECT
A7SEL ; A7/A8 PB HEAD SELECT
AUX1 - AUX3 ; MPX DATA AUXILIARY
B1SEL ; B1/B2 PB HEAD SELECT
B3SEL ; B3/B4 PB HEAD SELECT
B5SEL ; B5/B6 PB HEAD SELECT
B7SEL ; B7/B8 PB HEAD SELECT
CK51 ; 51.39 MHz REFERENCE CLOCK
CNFASEL, CNFBSEL ; CNF SYSTEM SELECT
DIVSEL ; MPX CLOCK DIVIDING RATIO SELECT (H : 1/4, L : 1/2)
DLENSEL ; MPX DATA LENGTH SELECT (H : 17-BIT, L : 8-BIT)
EXTSTP ; MPX DATA SYNC SYSTEM SELECT (H : INT, L : EXT)
FEEN ; FLYING ERASE HEAD CONTROL
RECSEL ; REC SYSTEM SELECT
STARTSEL ; MPX DATA EXTERNAL SYNC-LOCK
TEST ; TEST
$\overline{\text{XOEMPXD}}$ ; PE DATA AND PECK CONTROL
$\overline{\text{XRST}}$ ; SYSTEM RESET
YCASEL, YCBSEL ; ANALOG BETACAM PB Y/C HEAD SELECT

**OUTPUT**

CK13 ; 12.8 MHz CLOCK
$\overline{\text{CK13X}}$ ; PHASE INVERTED 12.8 MHz CLOCK
MPX ; BEFORE PRE-CODED MPX DATA
ODIVCK ; DOWN COUNTED (1/2 OR 1/4) MPX CLOCK
OSTP ; TIMING PULSE
PECK ; 25.7 MHz MPX CLOCK
PEDATA ; PRE-CODED MPX DATA


XOEMPXD
51
YCASEL
63
YCBSEL
64
RECSEL
1
AUX1
2
CNFASEL
3
CNFBSEL
4
FEEN
5
AUX2
6
A1SEL
7
A3SEL
8
A5SEL
9
A7SEL
11
AUX3
12
B1SEL
13
B3SEL
14
B5SEL
15
B7SEL
16
LATCH
17
HEAD PATTERN
PARITY
TAIL PATTERN
PARALLEL TO SERIAL CONVERTER
PRE-CODE
19
PEDATA
34
MPX
36
ODIVCK
DIVSEL
55
1/2 OR 1/4 DIVIDER
22
PECK
DLENSEL
56
8-BIT OR 17-BIT SELECTOR
EXTSTP
61
STARTSEL
54
EXT/INT SELECTOR
38
OSTP
CK51
60
1/2 DIVIDER
1/2 DIVIDER
46
CK13
44
CK13X
XRST
62