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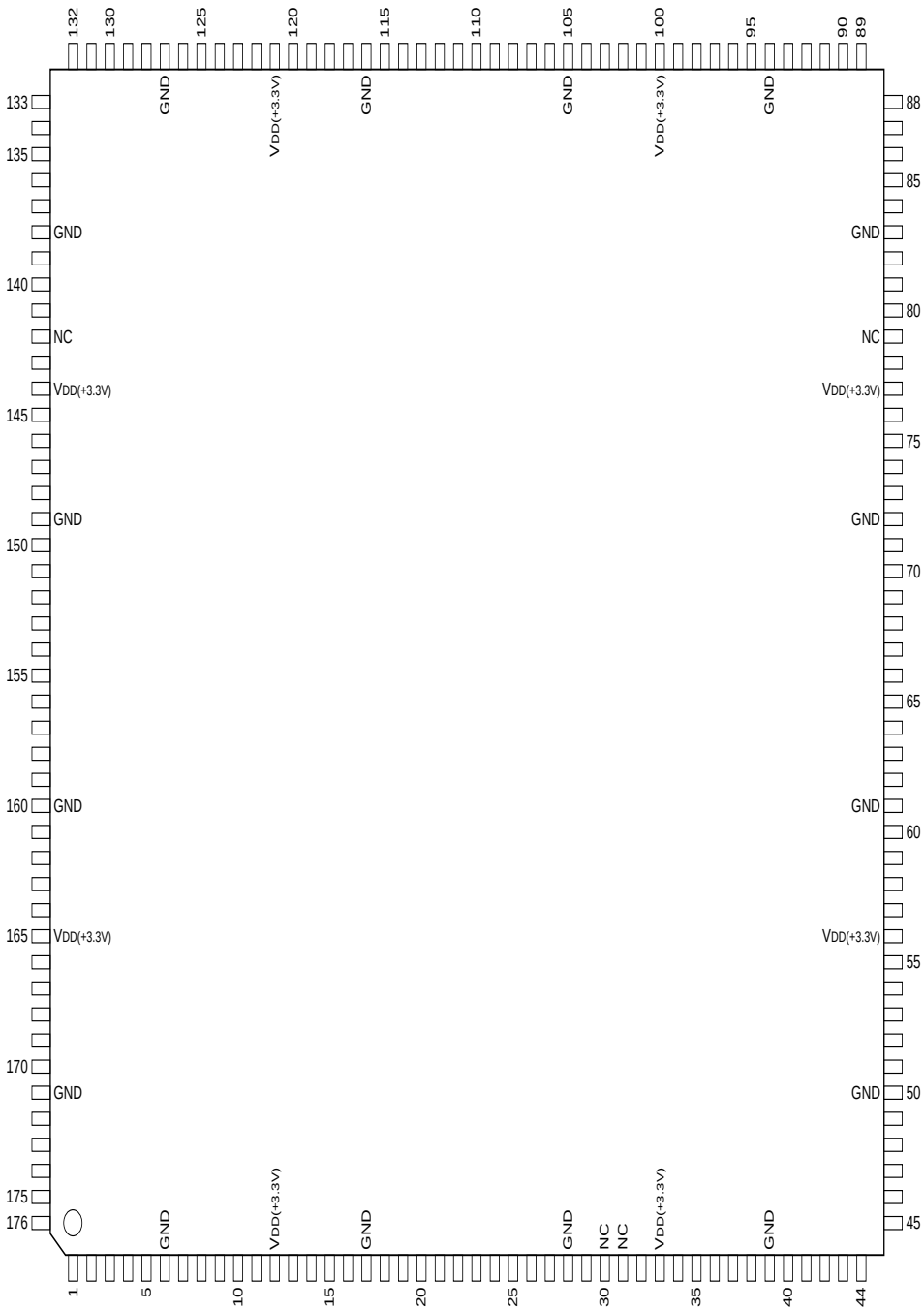
C-MOS GOP-DATA SORTER

–TOP VIEW–



(V_{DD} = +3.3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	IN1P	45	O	FO30	89	O	NTPO2	133	I	FI17
2	I	IN10	46	O	FO31	90	O	STPO2	134	I	FI16
3	I	IN11	47	O	FO32	91	O	OUT27	135	I	FI15
4	I	IN12	48	O	FO33	92	O	OUT26	136	I	FI14
5	I	IN13	49	O	FO34	93	O	OUT25	137	I	FI13
6	—	GND	50	—	GND	94	—	GND	138	—	GND
7	I	IN14	51	O	FO35	95	O	OUT24	139	I	FI12
8	I	IN15	52	O	FO36	96	O	OUT23	140	I	FI11
9	I	IN16	53	O	FO37	97	O	OUT22	141	I	FI10
10	I	IN17	54	O	FO40	98	O	OUT21	142	—	NC
11	I	STPI1	55	O	FO41	99	O	OUT20	143	O	FCK1
12	—	V_{DD}	56	—	V_{DD}	100	—	V_{DD}	144	—	V_{DD}
13	I	XSM	57	O	FO42	101	O	OUT2P	145	I	XMM
14	I	XMS	58	O	FO43	102	I/O	SE2	146	I	TCK
15	I	STAT0	59	O	FO44	103	I/O	GOP2	147	I	XWE
16	I	STAT1	60	O	FO45	104	I	XTST	148	I	CK
17	—	GND	61	—	GND	105	—	GND	149	—	GND
18	I	CS	62	O	FO46	106	I	TUD	150	O	RRST2
19	I	STRB	63	O	FO47	107	I	SDI0	151	O	RRST1
20	I/O	SYIO0	64	O	WE3	108	I	SDI1	152	O	WRST2
21	I/O	SYIO1	65	O	WE4	109	O	SDO0	153	O	WRST1
22	I/O	SYIO2	66	O	TE3	110	O	SDO1	154	O	RE2
23	I/O	SYIO3	67	O	TE4	111	I	TST0	155	O	RE1
24	I/O	SYIO4	68	O	RE3	112	I	TST1	156	O	WE2
25	I/O	SYIO5	69	O	RE4	113	I	TST2	157	O	WE1
26	I/O	SYIO6	70	O	WRST3	114	I	TST3	158	O	FO27
27	I/O	SYIO7	71	O	WRST4	115	I	TST4	159	O	FO26
28	—	GND	72	—	GND	116	—	GND	160	—	GND
29	I	NTPI	73	O	TRST3	117	I	TST5	161	O	FO25
30	—	NC	74	O	TRST4	118	I/O	SE1	162	O	FO24
31	—	NC	75	O	RRST3	119	I/O	GOP1	163	O	FO23
32	I	CLR	76	O	RRST4	120	O	NTPO1	164	O	FO22
33	—	V_{DD}	77	—	V_{DD}	121	—	V_{DD}	165	—	V_{DD}
34	I	IN2P	78	O	FCK2	122	O	STPO1	166	O	FO21
35	I	IN20	79	—	NC	123	O	OUT17	167	O	FO20
36	I	IN21	80	I	FI20	124	O	OUT16	168	O	FO17
37	I	IN22	81	I	FI21	125	O	OUT15	169	O	FO16
38	I	IN23	82	I	FI22	126	O	OUT14	170	O	FO15
39	—	GND	83	—	GND	127	—	GND	171	—	GND
40	I	IN24	84	I	FI23	128	O	OUT13	172	O	FO14
41	I	IN25	85	I	FI24	129	O	OUT12	173	O	FO13
42	I	IN26	86	I	FI25	130	O	OUT11	174	O	FO12
43	I	IN27	87	I	FI26	131	O	OUT10	175	O	FO11
44	I	STPI2	88	I	FI27	132	O	OUT1P	176	O	FO10

INPUT

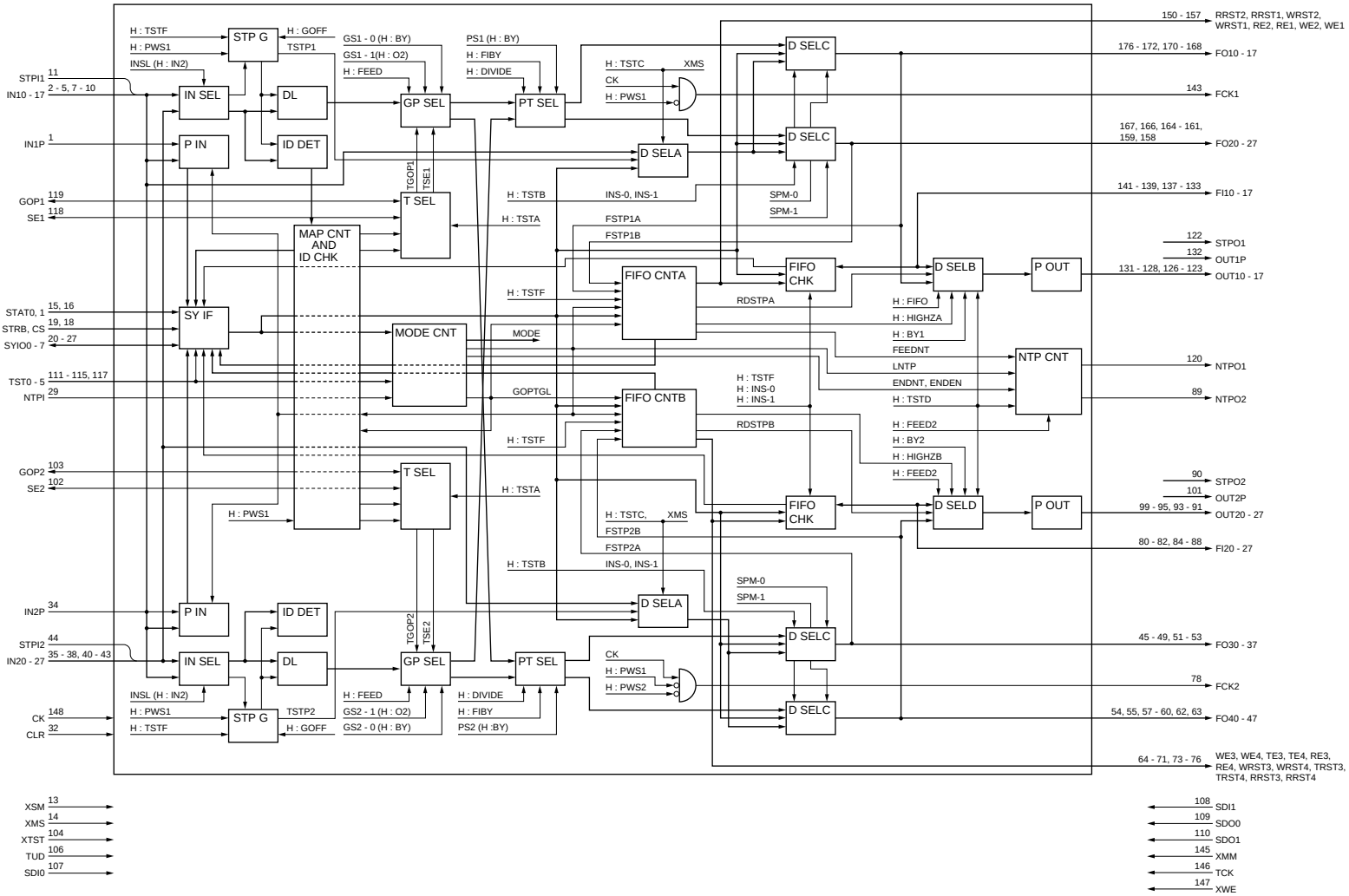
CK	;	27 MHz SYSTEM CLOCK
CLR	;	INTERNAL FLIP-FLOP CLEAR
CS	;	CHIP SELECT
FI10 - FI17	;	DATA INPUTS FROM FIFO 1 AND FIFO 2
FI20 - FI27	;	DATA INPUTS FROM FIFO 5 AND FIFO 6
IN10 - IN17	;	DATA INPUTS FROM INNER1
IN1P	;	PARITY BIT INPUT FROM INNER1
IN20 - IN27	;	DATA INPUTS FROM INNER2
IN2P	;	PARITY BIT INPUT FROM INNER2
NTPI	;	NON-TRACKING PULSE FROM SERVO
SDI0, SDI1	;	SCAN TEST DATA INPUTS
STAT0, STAT1	;	STATUS BITS
STPI1	;	START PULSE FROM INNER1
STPI2	;	START PULSE FROM INNER2
STRB	;	STROBE PULSE
TCK	;	INTERNAL RAM TEST CLOCK
TST0 - TST5	;	TEST SETTING BITS
TUD	;	PULL-UP/PULL-DOWN RESISTOR ON/OFF
XMM	;	INTERNAL RAM TEST MODE
XMS	;	SCAN PULSE SELECT
XSM	;	SCAN MODE (L : SCAN, H : NORMAL)
XTST	;	TEST MODE SIGNAL
XWE	;	INTERNAL RAM TEST WRITE ENABLE

OUTPUT

FCK1	;	WRITE/READ CLOCK OF FIFO 1 AND FIFO 2
FCK2	;	WRITE/READ CLOCK OF FIFO 3 TO FIFO 6
FO10 - FO17	;	DATA OUTPUTS TO FIFO 1
FO20 - FO27	;	DATA OUTPUTS TO FIFO 2
FO30 - FO37	;	DATA OUTPUTS TO FIFO 3
FO40 - FO47	;	DATA OUTPUTS TO FIFO 4
NTPO1	;	NON-TRACKING PULSE TO OUTER 1
NTPO2	;	NON-TRACKING PULSE TO OUTER 2
OUT10 - OUT17	;	DATA OUTPUTS TO OUTER 1
OUT1P	;	PARITY BIT OUTPUT TO OUTER 1
OUT20 - OUT27	;	DATA OUTPUTS TO OUTER 2
OUT2P	;	PARITY BIT OUTPUT TO OUTER 2
RE1	;	READ ENABLE PULSE OF FIFO 1
RE2	;	READ ENABLE PULSE OF FIFO 2
RE3	;	READ ENABLE PULSE OF FIFO 5
RE4	;	READ ENABLE PULSE OF FIFO 6
RRST1	;	READ RESET PULSE OF FIFO 1
RRST2	;	READ RESET PULSE OF FIFO 2
RRST3	;	READ RESET PULSE OF FIFO 5
RRST4	;	READ RESET PULSE OF FIFO 6
SDO0, SDO1	;	SCAN TEST DATA OUTPUTS
STPO1	;	START PULSE TO OUTER 1
STPO2	;	START PULSE TO OUTER 2
TE3	;	READ ENABLE PULSE OF FIFO 3 / WRITE ENABLE PULSE OF FIFO 5
TE4	;	READ ENABLE PULSE OF FIFO 4 / WRITE ENABLE PULSE OF FIFO 6
TRST3	;	READ RESET PULSE OF FIFO 3 / WRITE REST PULSE OF FIFO 5
TRST4	;	READ RESET PULSE OF FIFO 4 / WRITE REST PULSE OF FIFO 6
WRST1	;	WRITE RESET PULSE OF FIFO 1
WRST2	;	WRITE RESET PULSE OF FIFO 2
WRST3	;	WRITE RESET PULSE OF FIFO 3
WRST4	;	WRITE RESET PULSE OF FIFO 4
WE1	;	WRITE ENABLE PULSE OF FIFO 1
WE2	;	WRITE ENABLE PULSE OF FIFO 2
WE3	;	WRITE ENABLE PULSE OF FIFO 3
WE4	;	WRITE ENABLE PULSE OF FIFO 4

INPUT/OUTPUT

GOP1	;	GOP SELECT SIGNAL OF INNER 1
GOP2	;	GOP SELECT SIGNAL OF INNER 2
SE1	;	SYNC ENABLE SIGNAL OF INNER 1
SE2	;	SYNC ENABLE SIGNAL OF INNER 2
SYIO0 - SYIO7	;	SYSTEM CONTROL DATA BUS


STPI1
11
IN10 - 17
2 - 5, 7 - 10
IN1P
1
GOP1
119
SE1
118
STAT0, 1
15, 16
STRB, CS
19, 18
SYIO0 - 7
20 - 27
TST0 - 5
111 - 115, 117
NTPI
29
GOP2
103
SE2
102
IN2P
34
STPI2
44
IN20 - 27
35 - 38, 40 - 43
CK
148
CLR
32
XSM
13
XMS
14
XTST
104
TUD
106
SDI0
107
STP G
H : TSTF
H : PWS1
INSL (H : IN2)
H : GOFF
TSTP1
IN SEL
P IN
DL
ID DET
MAP CNT AND ID CHK
SY IF
MODE CNT
T SEL
GP SEL
PT SEL
GS1 - 0 (H : BY)
GS1 - 1(H : O2)
H : FEED
PS1 (H : BY)
H : FIBY
H : DIVIDE
TGOP1
TSE1
D SELA
H : TSTC
XMS
CK
H : PWS1
D SELC
H : TSTB
INS-0, INS-1
H : TSTA
FSTP1A
FSTP1B
SPM-0
SPM-1
FIFO CNTA
FIFO CHK
RDSTPA
MODE
GOPTGL
FIFO CNTB
RDSTPB
H : TSTF
H : INS-0
H : INS-1
H : PWS1
H : TSTC,
FSTP2B
FSTP2A
D SELB
D SELD
P OUT
H : FIFO
H : HIGHZA
H : BY1
FEEDNT
LNTP
ENDNT, ENDEN
H : TSTD
H : FEED2
H : BY2
H : HIGHZB
NTP CNT
TSTP2
GS2 - 1 (H : O2)
GS2 - 0 (H : BY)
PS2 (H :BY)
150 - 157
RRST2, RRST1, WRST2, WRST1, RE2, RE1, WE2, WE1
176 - 172, 170 - 168
FO10 - 17
143
FCK1
167, 166, 164 - 161, 159, 158
FO20 - 27
141 - 139, 137 - 133
FI10 - 17
122
STPO1
132
OUT1P
131 - 128, 126 - 123
OUT10 - 17
120
NTPO1
89
NTPO2
90
STPO2
101
OUT2P
99 - 95, 93 - 91
OUT20 - 27
80 - 82, 84 - 88
FI20 - 27
45 - 49, 51 - 53
FO30 - 37
78
FCK2
54, 55, 57 - 60, 62, 63
FO40 - 47
64 - 71, 73 - 76
WE3, WE4, TE3, TE4, RE3, RE4, WRST3, WRST4, TRST3, TRST4, RRST3, RRST4
108
SDI1
109
SDO0
110
SDO1
145
XMM
146
TCK
147
XWE