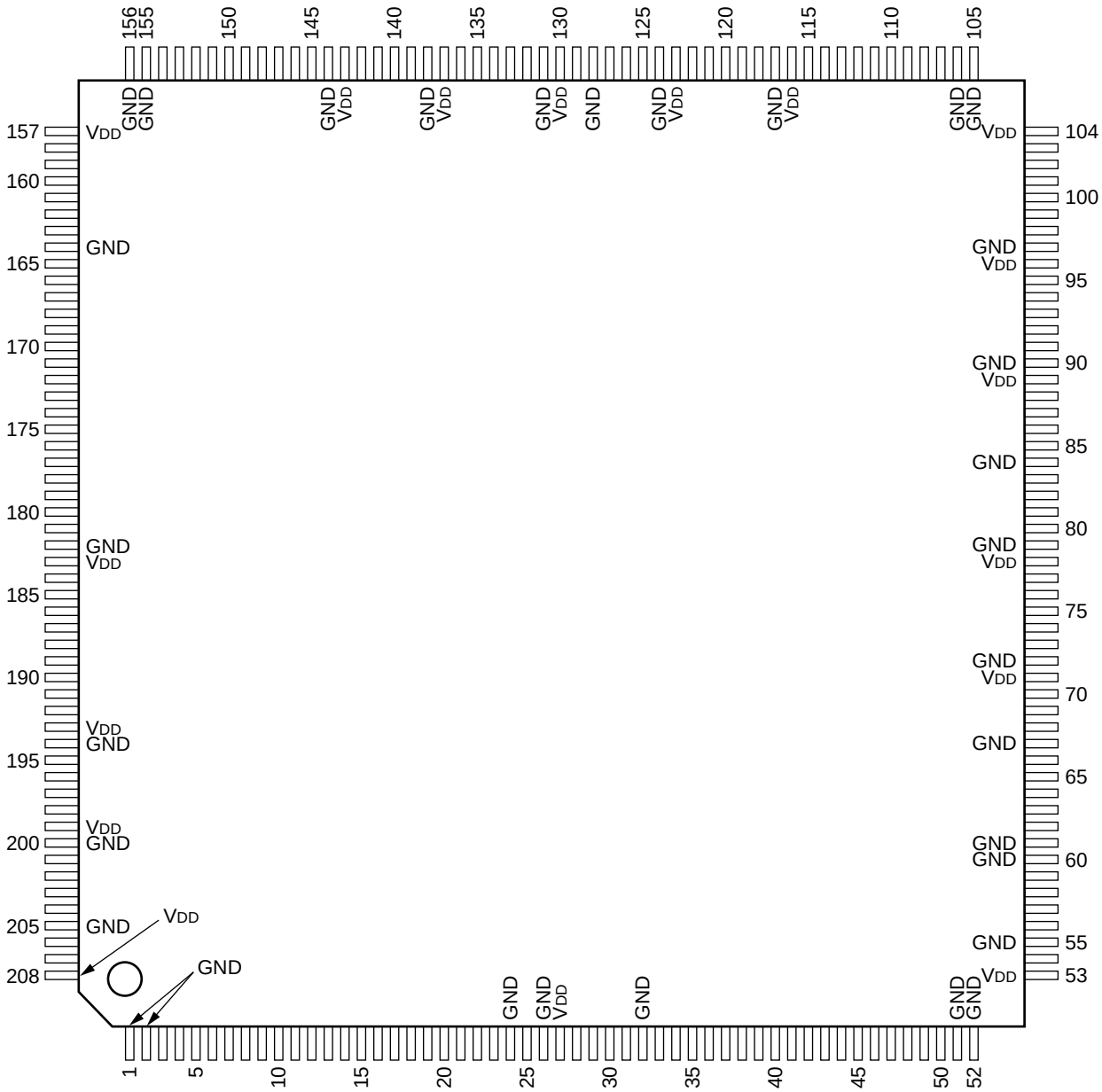
C-MOS ECC OUTER DECODER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	53	—	V_{DD}	105	—	GND	157	—	V_{DD}
2	—	GND	54	I	CK27	106	—	GND	158	O	OBSY
3	I	AREID0	55	—	GND	107	I	MDTES1	159	I	$\overline{\text{RSTRT}}$
4	I	AREID1	56	I	NTPLS	108	I	MDTES2	160	O	TESO0
5	I	SMC	57	I	DIN0	109	I	MDTES3	161	O	TESO1
6	I	SIN	58	I	DIN1	110	I	MDTES4	162	I	$\overline{\text{DECFR}}$
7	O	SOT	59	I	DIN2	111	O	JADRS0	163	O	$\overline{\text{SYNCO}}$
8	I	AREID2	60	—	GND	112	O	JADRS1	164	—	GND
9	I/O	SYSIO0	61	—	GND	113	O	JADRS2	165	O	DOUT0
10	I/O	SYSIO1	62	I	DIN3	114	O	JADRS3	166	O	DOUT1
11	I/O	SYSIO2	63	I	DIN4	115	O	JADRS4	167	O	DOUT2
12	I/O	SYSIO3	64	I	DIN5	116	—	V_{DD}	168	O	DOUT3
13	I/O	SYSIO4	65	I	DIN6	117	—	GND	169	O	DOUT4
14	I/O	SYSIO5	66	I	DIN7	118	O	JADRS5	170	O	DOUT5
15	I/O	SYSIO6	67	—	GND	119	O	JADRS6	171	O	DOUT6
16	I/O	SYSIO7	68	I/O	NIODT0	120	O	JADRS7	172	O	DOUT7
17	I	IBUSEN	69	I/O	NIODT1	121	O	JADRS8	173	I	TMC1
18	O	OBUSEN	70	I/O	NIODT2	122	O	JADRS9	174	I	TMC2
19	I	$\overline{\text{VD}}$	71	—	V_{DD}	123	—	V_{DD}	175	O	EFLGO
20	I	STAT0	72	—	GND	124	—	GND	176	O	PRTYO
21	I	STAT1	73	I/O	NIODT3	125	O	JADRS10	177	O	$\overline{\text{FRMST}}$
22	I	$\overline{\text{STRB}}$	74	I/O	NIODT4	126	O	JADRS11	178	O	$\overline{\text{GOPST}}$
23	I	$\overline{\text{CS}}$	75	I/O	NIODT5	127	O	$\overline{\text{JCKE}}$	179	O	CYCID0
24	—	GND	76	I/O	NIODT6	128	—	GND	180	O	CYCID1
25	I	$\overline{\text{RESET}}$	77	I/O	NIODT7	129	I	CK54	181	O	CYCID2
26	—	GND	78	—	V_{DD}	130	—	V_{DD}	182	—	GND
27	—	V_{DD}	79	—	GND	131	—	GND	183	—	V_{DD}
28	I	SCK	80	O	$\overline{\text{NWEN}}$	132	O	$\overline{\text{JWEN}}$	184	O	TOUT0
29	I	AMC	81	O	$\overline{\text{NRAS}}$	133	O	$\overline{\text{JRAS}}$	185	O	TOUT1
30	I	BUNRI	82	O	$\overline{\text{NCAS}}$	134	O	$\overline{\text{JCAS}}$	186	O	TOUT2
31	I	TEST	83	O	$\overline{\text{NCKE}}$	135	O	$\overline{\text{JCS0}}$	187	O	TOUT3
32	—	GND	84	—	GND	136	O	$\overline{\text{JCS1}}$	188	O	TOUT4
33	I	TIN0	85	O	$\overline{\text{NCS}}$	137	—	V_{DD}	189	O	TOUT5
34	I	TIN1	86	O	$\overline{\text{NDQM}}$	138	—	GND	190	O	TOUT6
35	I	TIN2	87	O	NADRS0	139	O	$\overline{\text{JDQM}}$	191	O	TOUT7
36	I	TIN3	88	O	NADRS1	140	I/O	JIODT0	192	O	TOUT8
37	I	TIN4	89	—	V_{DD}	141	I/O	JIODT1	193	—	V_{DD}
38	I	TIN5	90	—	GND	142	I/O	JIODT2	194	—	GND
39	I	TIN6	91	O	NADRS2	143	—	V_{DD}	195	O	AU 1/2
40	I	TIN7	92	O	NADRS3	144	—	GND	196	O	AU 3/4
41	I	TIN8	93	O	NADRS4	145	I/O	JIODT3	197	O	$\overline{\text{AVSTO}}$
42	I	TIN9	94	O	NADRS5	146	I/O	JIODT4	198	O	SWFS
43	I	TIN10	95	O	NADRS6	147	I/O	JIODT5	199	—	V_{DD}
44	I	TIN11	96	—	V_{DD}	148	I/O	JIODT6	200	—	GND
45	I	TIN12	97	—	GND	149	I/O	JIODT7	201	I	FS512
46	I	TIN13	98	O	NADRS7	150	I	XMOD1	202	O	DEAUID0
47	I	XMOD0	99	O	NADRS8	151	I	SVBNK0	203	O	DEAUID1
48	I	$\overline{\text{REV}}$	100	O	NADRS9	152	I	SVBNK1	204	O	DEAUID2
49	I	PRITY	101	O	NADRS10	153	I	SVBNK2	205	—	GND
50	I	$\overline{\text{SYNC}}$	102	O	NADRS11	154	I	SVBNK3	206	I	$\overline{\text{AREFV}}$
51	—	GND	103	I	MDTES0	155	—	GND	207	I	FS
52	—	GND	104	—	V_{DD}	156	—	GND	208	—	V_{DD}

INPUT

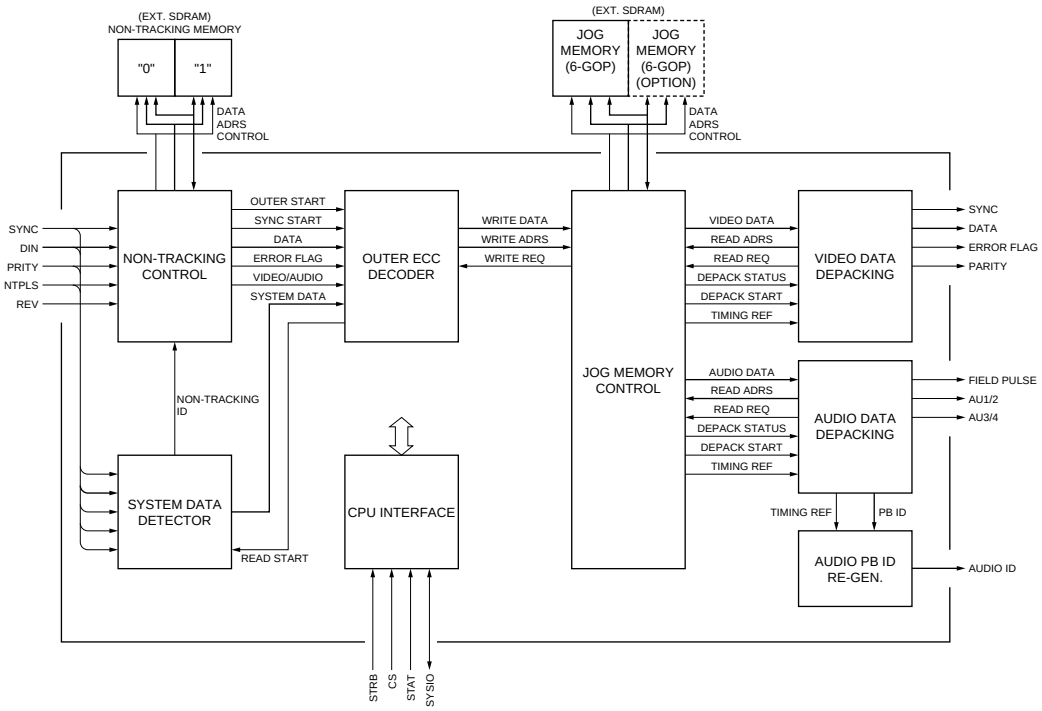
AMC	;	ATG MODE CONTROL
AREFV	;	AUDIO REFERENCE V
AREID0 - AREID2	;	AUDIO REFERENCE ID
BUNRI	;	RAM RELEASE TEST
CK27	;	27 MHz CLOCK
CK54	;	54 MHz CLOCK
CS	;	CPU INTERFACE CHIP SELECT
DECFR	;	DECODE FRAME
DIN0 - DIN7	;	DATA
FS	;	FS
FS512	;	512fs CLOCK
IBUSEN	;	CPU I/F DATA BUS OUTPUT ENABLE
MDTES0 - MDTES4	;	TEST MODE
NTPLS	;	NON-TRACKING PULSE
PRITY	;	PARITY
REEST	;	POWER ON RESET
REV	;	CAPSTAN FWD/REV (L : FWD, H : REV)
RSTRT	;	JOG MEMORY READ START
SCK	;	SCAN CLOCK
SIN	;	TEST (SCAN CHECK)
SMC	;	TEST (SCAN CHECK)
STAT0, STAT1	;	CPU INTERFACE STAT
STRB	;	CPU INTERFACE STROBE
SVBNK0 - SVBNK3	;	JOG MEMORY BANK CONTROL
SYNC	;	INNER SYNC
TEST	;	RAM TEST MODE
TIN0 - TIN13	;	TEST DATA
TMC1, TMC2	;	TEST MODE CONTROL
VD	;	VERTICAL DRIVE
XMOD0	;	SYSTEM AUXILIARY DETECT MODE
XMOD1	;	JOG MEMORY AUTO BANK MODE

OUTPUT

AU 1/2	;	CH-1/CH-2 SERIAL AUDIO DATA
AU 3/4	;	CH-3/CH-4 SERIAL AUDIO DATA
AVSTO	;	AUDIO FIELD START
CYCID0 - CYCID2	;	CYCLIC ID
DEAUID0 - DEAUID2	;	DECODED AUDIO ID
DOUT0 - DOUT7	;	BIT RATE REDUCTION STREAM DATA
EFLGO	;	BIT RATE REDUCTION STREAM ERROR FLAG
FRMST	;	FRAME START PULSE
GOPST	;	GROUP OF PICTURE START PULSE
JADRS0 - JADRS11	;	ADDRESS BUS FOR JOG MEMORY SDRAM
JCAS	;	COLUMN ADDRESS STROBE FOR JOG MEMORY SDRAM
JCKE	;	CLOCK ENABLE FOR JOG MEMORY SDRAM
JCS0, JCS1	;	CHIP SELECT FOR JOG MEMORY SDRAM
JDQM	;	DATA MASK CONTROL FOR JOG MEMORY SDRAM
JRAS	;	RAW ADDRESS STROBE FOR JOG MEMORY SDRAM
JWEN	;	WRITE ENABLE FOR JOG MEMORY SDRAM
NADRS0 - NADRS11	;	ADDRESS BUS FOR NON-TRACKING SDRAM
NCAS	;	COLUMN ADDRESS STROBE FOR NON-TRACKING SDRAM
NCKE	;	CLOCK ENABLE FOR NON-TRACKING SDRAM
NCS	;	CHIP SELECT FOR NON-TRACKING SDRAM
NDQM	;	DATA MASK CONTROL FOR NON-TRACKING SDRAM
NRAS	;	RAW ADDRESS STROBE FOR NON-TRACKING SDRAM
NWEN	;	WRITE ENABLE FOR NON-TRACKING SDRAM
OBSY	;	JOG MEMORY READ BUSY
OBUSEN	;	CPU I/F DATA BUS OUTPUT ENABLE
PRTYO	;	BIT RATE REDUCTION STREAM PARITY
SOT	;	TEST (SCAN CHECK)
SWFS	;	FS
SYNCO	;	BIT RATE REDUCTION STREAM SYNC
TESO0, TESO1	;	TEST DATA
TOUT0, TOUT8	;	TEST DATA

INPUT/OUTPUT

JIODT0 - JIODT7	;	DATA BUS FOR JOG MEMORY SDRAM
NIODT0 - NIODT7	;	DATA BUS FOR NON-TRACKING SDRAM
SYSIO0 - SYSIO7	;	CPU INTERFACE DATA BUS


(EXT. SDRAM)
NON-TRACKING MEMORY
"0"
"1"
DATA
ADRS
CONTROL
(EXT. SDRAM)
JOG MEMORY (6-GOP)
JOG MEMORY (6-GOP) (OPTION)
DATA
ADRS
CONTROL
SYNC
DIN
PRITY
NTPLS
REV
NON-TRACKING CONTROL
OUTER START
SYNC START
DATA
ERROR FLAG
VIDEO/AUDIO
SYSTEM DATA
OUTER ECC DECODER
WRITE DATA
WRITE ADRS
WRITE REQ
JOG MEMORY CONTROL
VIDEO DATA
READ ADRS
READ REQ
DEPACK STATUS
DEPACK START
TIMING REF
VIDEO DATA DEPACKING
SYNC
DATA
ERROR FLAG
PARITY
AUDIO DATA
READ ADRS
READ REQ
DEPACK STATUS
DEPACK START
TIMING REF
AUDIO DATA DEPACKING
FIELD PULSE
AU1/2
AU3/4
TIMING REF
PB ID
AUDIO PB ID RE-GEN.
AUDIO ID
NON-TRACKING ID
SYSTEM DATA DETECTOR
READ START
CPU INTERFACE
STRB
CS
STAT
SYSIO