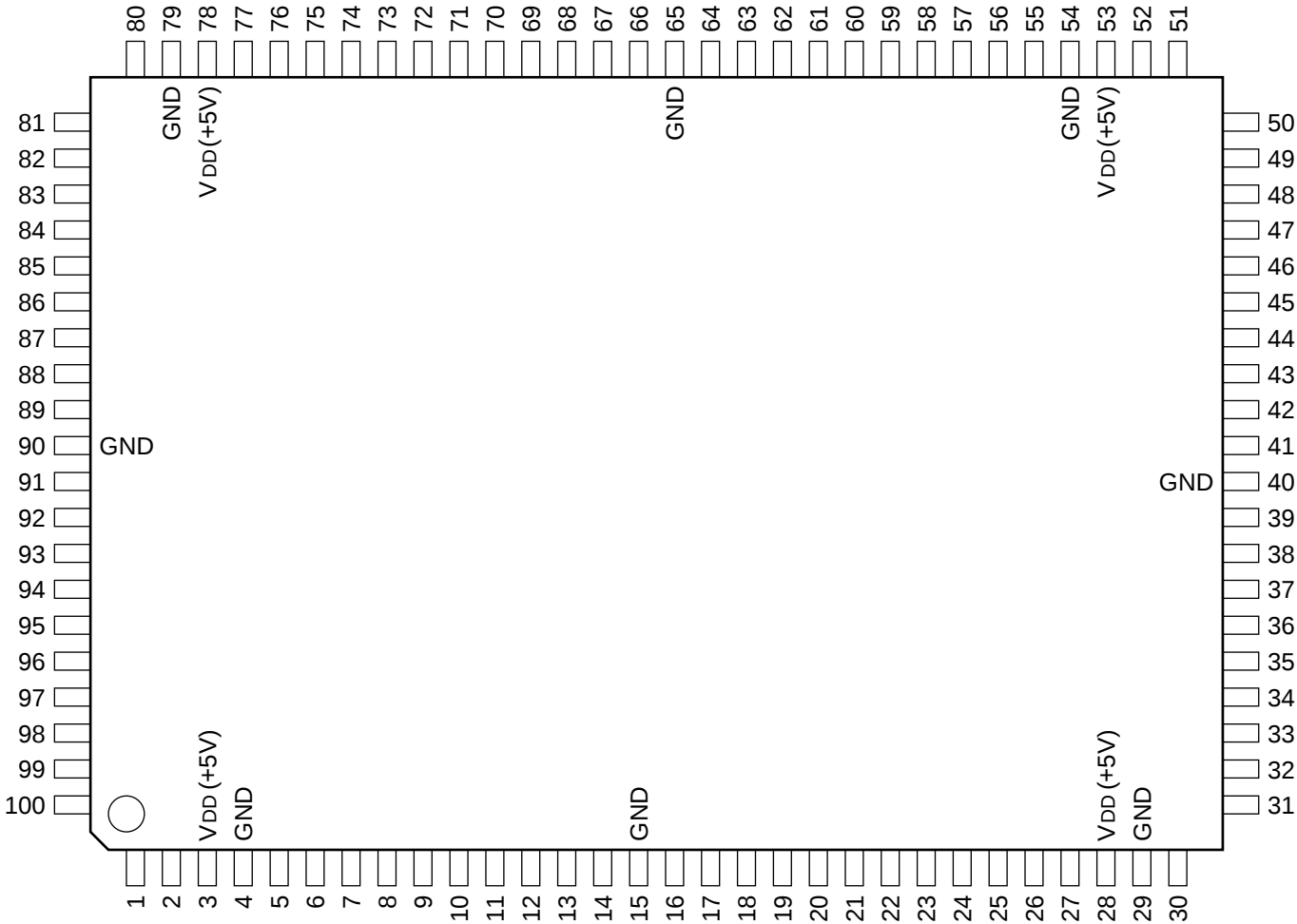

C-MOS ADDRESS ARITHMETIC PROCESSOR

- TOP VIEW -



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	AUX5	26	I	D9	51	O	T11	76	O	N5
2	O	AUX4	27	I	D8	52	O	T10	77	O	N4
3	–	V _{DD}	28	–	V _{DD}	53	–	V _{DD}	78	–	V _{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	O	AUX3	30	I	D7	55	O	T9	80	O	N3
6	O	AUX2	31	I	D6	56	O	T8	81	O	N2
7	O	AUX1	32	I	D5	57	O	T7	82	O	N1
8	I	C2	33	I	D4	58	O	T6	83	O	N0
9	I	C1	34	I	D3	59	O	T5	84	I	LN0
10	I	C0	35	I	D2	60	O	T4	85	I	AR1
11	I	TSL	36	I	D1	61	O	T3	86	I	AR0
12	O	AUX0	37	I	D0	62	O	T2	87	O	ER
13	O	TCE1	38	I	WE2	63	O	T1	88	O	E4
14	O	TCE0	39	I	WE1	64	O	T0	89	O	E3
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	TWE1	41	I	CK	66	O	N15	91	O	E2
17	O	TWE0	42	I	WE0	67	O	N14	92	O	E1
18	O	TLT	43	I	A3	68	O	N13	93	O	E0
19	I	TWT	44	I	A2	69	O	N12	94	I	CE
20	I	D15	45	I	A1	70	O	N11	95	I	C7
21	I	D14	46	I	MODE	71	O	N10	96	I	C6
22	I	D13	47	O	T15	72	O	N9	97	I	C5
23	I	D12	48	O	T14	73	O	N8	98	I	C4
24	I	D11	49	O	T13	74	O	N7	99	I	C3
25	I	D10	50	O	T12	75	O	N6	100	O	AUX6

45			83	
44	A1	N0	82	
43	A2	N1	81	
	A3	N2	80	
		N3	77	
37	D0	N4	76	
36	D1	N5	75	
35	D2	N6	74	INPUT
34	D3	N7	73	A1-A3 ; ADDRESS
33	D4	N8	72	AR0, AR1 ; FP (FRONT PROCESSOR) CONTROL SIGNAL (AREA) AT
32	D5	N9	71	COMMAND INTERFACE MODE
31	D6	N10	70	C0-C7 ; FP (FRONT PROCESSOR) CONTROL COMMAND AT
30	D7	N11	69	COMMAND DIRECT MODE
27	D8	N12	68	CE ; FP (FRONT PROCESSOR) CONTROL COMMAND ENABLE
26	D9	N13	67	CK ; CLOCK
25	D10	N14	66	D0-D15 ; DATA
24	D11	N15	64	LN0 ; FP (FRONT PROCESSOR) CONTROL SIGNAL (LINE) AT
23	D12		63	COMMAND INTERFACE MODE
22	D13	T0	62	MODE ; OPERATING MODE SELECT
21	D14	T1	61	TSL ; TABLE RAM BANK SELECT
20	D15	T2	60	TWT ; TABLE RAM WRITE TRIGGER
		T3	59	WE0-WE2 ; WRITE ENABLE
42	WE0	T4	58	
39	WE1	T5	57	OUTPUT
38	WE2	T6	56	AUX ; GENERAL PURPOSE REGISTER DATA
		T7	55	E0-E4 ; EXPONENT PART DATA
84	LN0	T8	52	ER ; ARITHMETIC STATUS
		T9	51	N0-N15 ; N SYSTEM ARITHMETIC SIGNAL
86	AR0	T10	50	T0-T15 ; T SYSTEM ARITHMETIC SIGNAL
85	AR1	T11	49	TCE0, TCE1 ; TABLE RAM CHIP ENABLE
		T12	48	TLT ; TABLE RAM ADDRESS AND DATA BUS LACH
94	CE	T13	47	TWE0, TWE1 ; TABLE RAM WRITE ENABLE
		T14	87	
10	C0	T15	93	
9	C1	ER	92	
8	C2	E0	91	
99	C3	E1	89	
98	C4	E2	88	
97	C5	E3	12	
96	C6	E4	7	
95	C7	AUX0	6	
		AUX1	5	
		AUX2	2	
		AUX3	1	
		AUX4	100	
		AUX5	18	
		AUX6	14	
19	TWT	TLT	13	
11	TSL	TCE0	17	
		TCE1	16	
46	MOD	TWE0		
41	>	TWE1		

