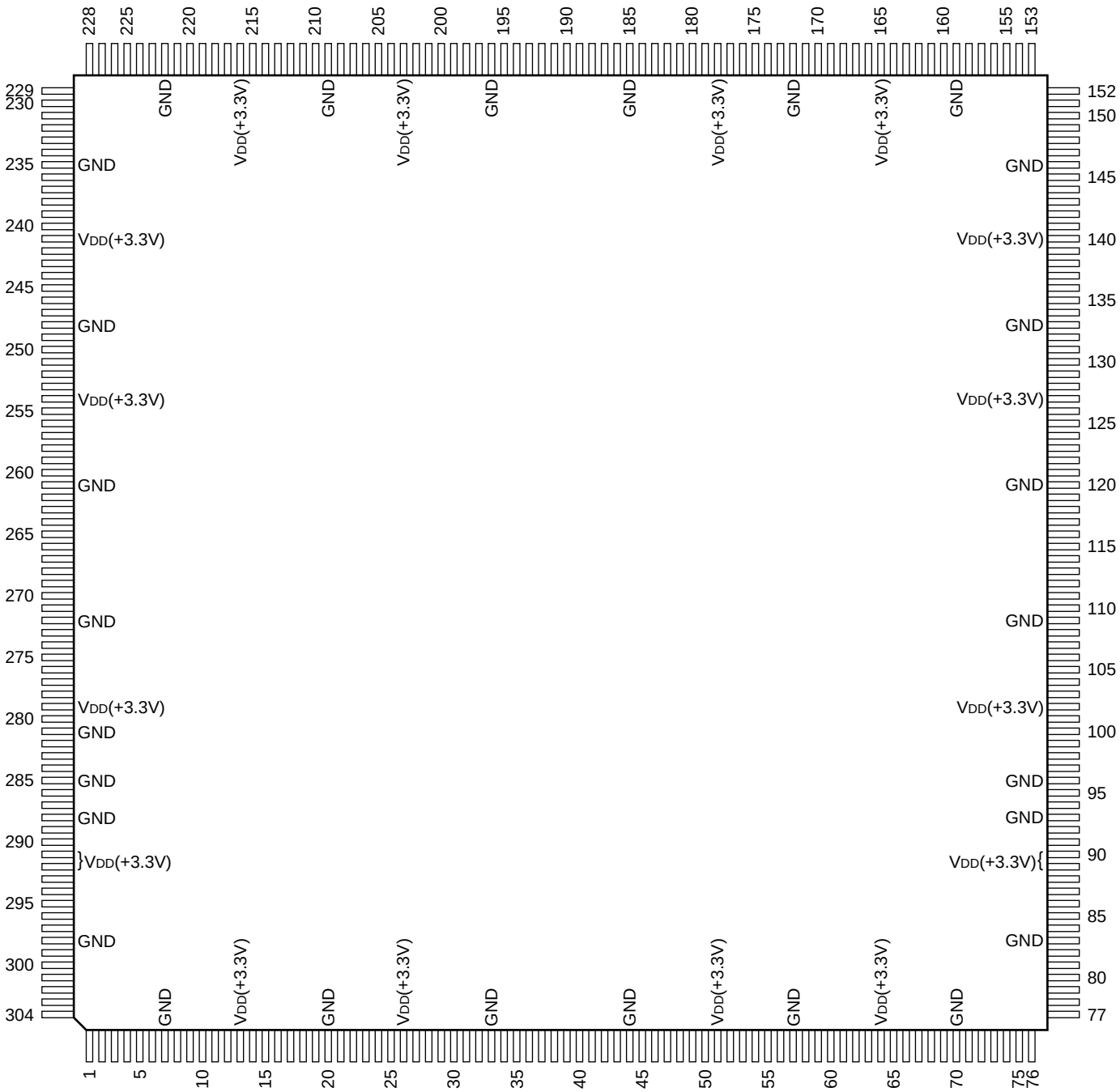
****

IL08

C-MOS INNER ERROR CORRECTION DECODER

– TOP VIEW –



(V_{DD} =+3.3V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	ADVDB4	62	I	REC	123	I/O	MEMA1D1	184	O	VADATA4	245	O	MB2AD2
2	I	CNFDB0	63	O	DHBDSW	124	I/O	MEMA1D2	185	–	GND	246	O	MB2AD1
3	I	CNVDB1	64	–	V_{DD}	125	I/O	MEMA1D3	186	O	VADATA5	247	O	MB2AD0
4	I	CNFDB2	65	I	ADVDA0	126	I/O	MEMA1D4	187	O	VADATA6	248	–	GND
5	I	CNFDB3	66	I	ADVDA1	127	–	V_{DD}	188	O	VADATA7	249	I	$\overline{\text{WECN2}}$
6	I	CNFDB4	67	I	ADVDA2	128	I/O	MEMA1D5	189	O	VADATA8	250	O	$\overline{\text{MBWE}}$
7	–	GND	68	I	ADVDA3	129	I/O	MEMA1D6	190	O	F5	251	I/O	MEMB1D7
8	I	RECDB0	69	I	ADVDA4	130	I/O	MEMA1D7	191	O	AUAXS	252	I/O	MEMB1D6
9	I	RECDB1	70	–	GND	131	O	$\overline{\text{MAWE}}$	192	O	AUCH	253	I/O	MEMB1D5
10	I	RECDB2	71	I	CNFDA0	132	I	$\overline{\text{WECN1}}$	193	O	AUSYNC	254	–	V_{DD}
11	I	RECDB3	72	I	CNFDA1	133	–	GND	194	O	AUST	255	I/O	MEMB1D4
12	I	RECDB4	73	I	CNFDA2	134	O	MA2AD0	195	O	VAPRITY	256	I/O	MEMB1D3
13	–	V_{DD}	74	I	CNFDA3	135	O	MA2AD1	196	–	GND	257	I/O	MEMB1D2
14	O	FS5F0	75	I	CNFDA4	136	O	MA2AD2	197	I/O	MAXB	258	I/O	MEMB1D1
15	O	FS5F1	76	I	RECDA0	137	O	MA2AD3	198	I/O	STLBD0	259	I/O	MEMB1D0
16	O	FS5F2	77	I	RECDA1	138	O	MA2AD4	199	I/O	STLBD1	260	O	MB1AD16
17	O	FSPRTY	78	I	RECDA2	139	O	MA2AD5	200	I/O	STLBD2	261	–	GND
18	O	RST	79	I	RECDA3	140	–	V_{DD}	201	I/O	STLBD3	262	O	MB1AD15
19	I/O	SYSIO0	80	I	RECDA4	141	O	MA2AD6	202	I/O	STLBD4	263	O	MB1AD14
20	–	GND	81	I	ADVSWA	142	O	MA2AD7	203	–	V_{DD}	264	O	MB1AD13
21	I/O	SYSIO1	82	I	ADVCKA	143	O	MA2AD8	204	I/O	STLBD5	265	O	MB1AD12
22	I/O	SYSIO2	83	–	GND	144	O	MA2AD9	205	I/O	STLBD6	266	O	MB1AD11
23	I/O	SYSIO3	84	I	CNFCKA	145	O	MA2AD10	206	I/O	STLBD7	267	O	MB1AD10
24	I/O	SYSIO4	85	I	TGTP1	146	–	GND	207	I/O	STLBD8	268	O	MB1AD9
25	I/O	SYSIO5	86	I	TGTP2	147	O	MA2AD11	208	I/O	MAXA	269	O	MB1AD8
26	–	V_{DD}	87	I	TGTP3	148	O	MA2AD12	209	–	GND	270	O	MB1AD7
27	I/O	SYSIO6	88	I	CNFSWA	149	O	MA2AD13	210	I/O	STLAD0	271	O	MB1AD6
28	I/O	SYSIO7	89	–	V_{DD}	150	O	MA2AD14	211	I/O	STLAD1	272	–	GND
29	I	GCTL0	90	–	V_{DD}	151	O	MA2AD15	212	I/O	STLAD2	273	O	MB1AD5
30	I	GCTL1	91	I	XMM	152	O	MA2AD16	213	I/O	STLAD3	274	O	MB1AD4
31	I	GCTL2	92	I	MCK	153	I/O	MEMA2D0	214	I/O	STLAD4	275	O	MB1AD3
32	I	GCTL3	93	–	GND	154	I/O	MEMA2D1	215	I/O	STLAD5	276	O	MB1AD2
33	–	GND	94	I	RECSWA	155	I/O	MEMA2D2	216	–	V_{DD}	277	O	MB1AD1
34	I	GCTL4	95	I	RECCKA	156	I/O	MEMA2D3	217	I/O	STLAD6	278	O	MB1AD0
35	I	GCTL5	96	–	GND	157	I/O	MEMA2D4	218	I/O	STLAD7	279	–	V_{DD}
36	I	STRB	97	O	WST1	158	I/O	MEMA2D5	219	I/O	STLAD8	280	O	$\overline{\text{MWR2}}$
37	I	SCS	98	I	REFV	159	–	GND	220	I/O	MEMB2D7	281	–	GND
38	I	STAT0	99	I	REFVP	160	I/O	MEMA2D6	221	I/O	MEMB2D6	282	I	CHSL
39	I	STAT1	100	I	SYTEST	161	I/O	MEMA2D7	222	–	GND	283	I	STTP
40	I	CHIPID0	101	O	$\overline{\text{MWR1}}$	162	I/O	DREFIO	223	I/O	MEMB2D5	284	O	WST2
41	I	CHIPID1	102	–	V_{DD}	163	I/O	WRIO	224	I/O	MEMB2D4	285	–	GND
42	I	GTEST	103	O	MA1AD0	164	O	VPRITY	225	I/O	MEMB2D3	286	I	RECCKB
43	I	$\overline{\text{RST3}}$	104	O	MA1AD1	165	–	V_{DD}	226	I/O	MEMB2D2	287	I	RECSWB
44	–	GND	105	O	MA1AD2	166	O	VBLK	227	I/O	MEMB2D1	288	–	GND
45	O	REVO	106	O	MA1AD3	167	O	VSYNC	228	I/O	MEMB2D0	289	I	PCK
46	O	JUMPO	107	O	MA1AD4	168	O	VVST	229	O	MB2AD16	290	I	MS
47	O	$\overline{\text{SHTLO}}$	108	O	MA1AD5	169	O	VDATA0	230	O	MB2AD15	291	–	V_{DD}
48	O	SEG0	109	–	GND	170	O	VDATA1	231	O	MB2AD14	292	–	V_{DD}
49	O	SEG1	110	O	MA1AD6	171	O	VDATA2	232	O	MB2AD13	293	I	CNFSWB
50	O	F0	111	O	MA1AD7	172	–	GND	233	O	MB2AD12	294	I	REV
51	–	V_{DD}	112	O	MA1AD8	173	O	VDATA3	234	O	MB2AD11	295	I	JUMP
52	O	TRREF	113	O	MA1AD9	174	O	VDATA4	235	–	GND	296	I	PULLTST
53	O	NOSIGO	114	O	MA1AD10	175	O	VDATA5	236	O	MB2AD10	297	I	CNFCKB
54	O	ACSY	115	O	MA1AD11	176	O	VDATA6	237	O	MB2AD9	298	–	GND
55	O	BDSY	116	O	MA1AD12	177	O	VDATA7	238	O	MB2AD8	299	I	ADVCKB
56	I	RST1	117	O	MA1AD13	178	–	V_{DD}	239	O	MB2AD7	300	I	ADVSWB
57	–	GND	118	O	MA1AD14	179	O	VDATA8	240	O	MB2AD6	301	I	ADVDB0
58	I	$\overline{\text{RST2}}$	119	O	MA1AD15	180	O	VADATA0	241	–	V_{DD}	302	I	ADVDB1
59	O	ACEF	120	–	GND	181	O	VADATA1	242	O	MB2AD5	303	I	ADVDB2
60	O	BDEF	121	O	MA1AD16	182	O	VADATA2	243	O	MB2AD4	304	I	ADVDB3
61	O	MON	122	I/O	MEMA1D0	183	O	VADATA3	244	O	MB2AD3			

INPUT

ADVCKA, ADVCKB	; ADVANCE A/C, B/D CH CLOCK
ADVDA0–ADVDA4, ADVDB0–ADVDB4	; ADVANCE A/C, B/D CH DATA
ADVSWA, ADVSWB	; ADVANCE A/C, B/D CH HEAD SWITCHING
CHIPID0, CHIPID1	; SYSTEM CONTROL INTERFACE CHIP ID
CHSL	; 1–4CH/5–8CH SELECT
CNFCKA, CNFCKB	; CONFIDENCE A/C, B/D CH CLOCK
CNFDA0–CNFDA4, CNFDB0–CNFDB4	; CONFIDENCE A/C, B/D CH DATA
CNFSWA, CNFSWB	; CONFIDENCE A/C, B/D CH HEAD SWITCHING
GCTL0–GCTL5, GTEST, PULLTST	; TEST PIN
JUMP	; DT JUMP
MCK	; 13.5 MHz CLOCK
MS	; SHUTTLE INTERFACE CONTROL
PCK	; 13.5 MHz PROGRAM PLAY CLOCK
REC	; RECORD MODE
RECCKA, RECCKB	; RECORD A/C, B/D CH CLOCK
RECDA0–RECDA4, RECDB0–RECDB4	; RECORD A/C, B/D CH DATA
RECSWA, RECSWB	; RECORD A/C, B/D CH HEAD SWITCHING SIGNAL
REFV	; REFERENCE VD
REFVP	; PROGRAM PLAY REFERENCE VD
REV	; REVERSE MODE INPUT
$\overline{\text{RST1}}$, $\overline{\text{RST2}}$, $\overline{\text{RST3}}$	; IC RESET 1.2.3
SCS	; SYSTEM CONTROL INTERFACE CHIP SELECT
STAT0, STAT1	; SYSTEM CONTROL INTERFACE STATES
STRB	; SYSTEM CONTROL INTERFACE STROBE
STTP, SYTEST, TGTP1–TGTP3, XMM	; TEST PIN
$\overline{\text{WECN1}}$, $\overline{\text{WECN2}}$	; A/C, B/D CH FIELD MEMORY DATA ENABLE

OUTPUT

ACEF, BDEF	; A/C, B/D CH ERROR FLAG
ACSY, BDSY	; A/C, B/D CH SYNC
AUAXS	; AUDIO AUXILIARY DATA SYNC PULSE
AUCH	; AUDIO CHANNEL PULSE
AUST	; AUDIO FIELD START PULSE
AUSYNC	; AUDIO SYNC PULSE
DHBDSW	; TEST PIN
F0	; FIELD ID
F5	; 526/60 AUDIO 0 FIELD PULSE
FS5F0–FS5F2	; AUDIO 5 FIELD SEQUENCE
FSPRTY	; AUDIO 5 FIELD SEQUENCE PARITY
JUMPO	; DT JUMP STATES
MA1AD0–MA1AD16, MB1AD0–MB1AD16	; A/C, B/D CH FIELD MEMORY 1 ADDRESS
MA2AD0–MA2AD16, MB2AD0–MB2AD16	; A/C, B/D CH FIELD MEMORY 2 ADDRESS
$\overline{\text{MAWE}}$, $\overline{\text{MBWE}}$	; A/C, B/D CH FIELD MEMORY WRITE ENABLE
MON	; TEST PIN
$\overline{\text{MWR1}}$, $\overline{\text{MWR2}}$	; A/C, B/D CH FIELD MEMORY WRITE/READ CONTROL
NOSIGO	; NO SIGNAL STATES
REVO	; REVERSE STATES
SEG0, SEG1	; SEGMENT NUMBER
$\overline{\text{SHTLO}}$	; SHUTTLE STATES
TRREF	; TRACK SYNC PULSE
VADATA0–VADATA8	; AUDIO DATA AND B/D CH VIDEO DATA
VAPRITY	; AUDIO VIDEO DATA PARITY
VBLK	; VIDEO ECC BLOCK PULSE
VDATA0–VDATA8	; A/C CH VIDEO DATA
VPRITY	; VIDEO DATA PARITY
VSYNC	; VIDEO SYNC PULSE
VVST	; VIDEO FIELD START PULSE
WST1, WST2	; TEST PIN

INPUT/OUTPUT

DREFIO	; REFERENCE VD SYNCHRONOUS INTERFACE
MAXA, MAXB	; A/C, B/D CH SHUTTLE OLD FLAG INTERFACE
MEMA1D0–MEMA1D7, MEMB1D0–MEMB1D7	; A/C, B/D CH FIELD MEMORY 1 DATA
MEMA2D0–MEMA2D7, MEMB2D0–MEMB2D7	; A/C, B/D CH FIELD MEMORY 2 DATA
STLAD0–STLAD8, STLBD0–STLBD8	; A/C, B/D CH SHUTTLE DATA INTERFACE
SYSIO0–SYSIO7	; SYSTEM CONTROL INTERFACE DATA
WRIO	; WRITE/READ CONTROL SYNCHRONOUS INTERFACE