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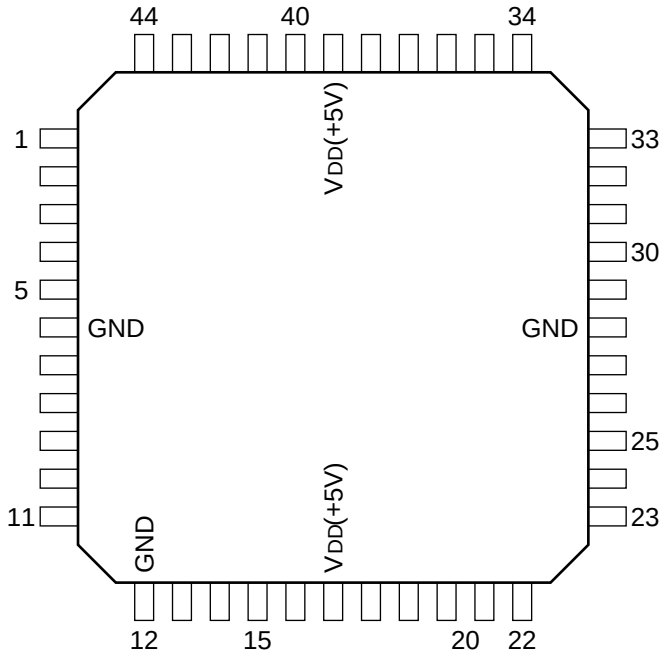
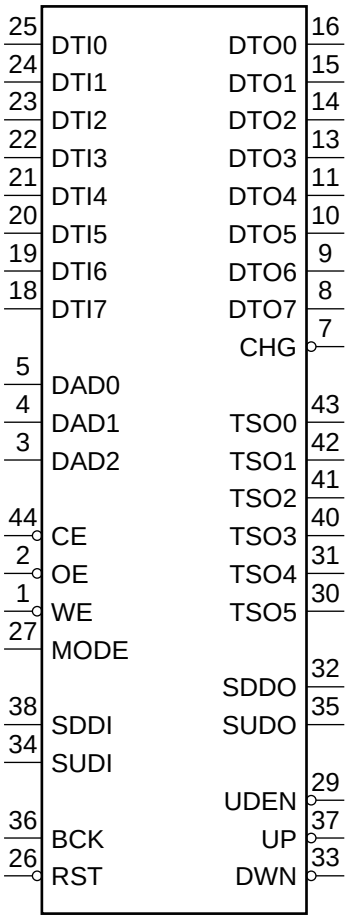
C-MOS DATA I/F For CONFERENCE SYSTEM

- TOP VIEW -





(V DD=+5V)

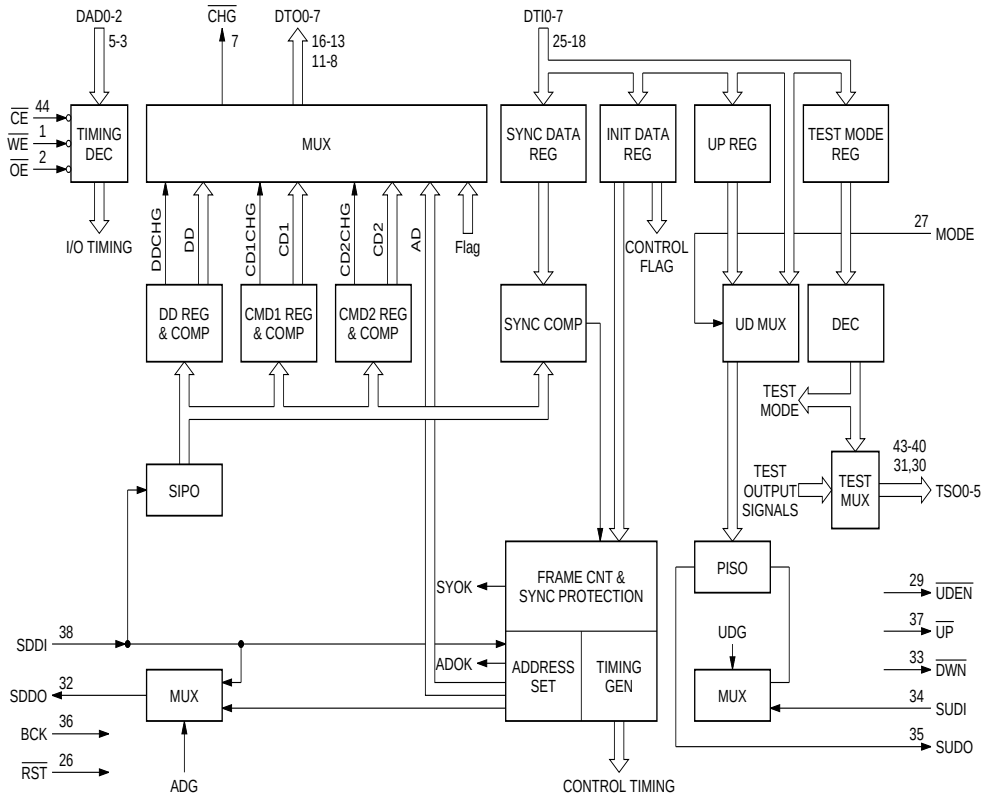
PIN No.	SYMBOL	I/O	PIN No.	SYMBOL	I/O
1	$\overline{WE}$	I	23	DTI2	I
2	$\overline{OE}$	I	24	DTI1	I
3	DAD2	I	25	DTI0	I
4	DAD1	I	26	$\overline{RST}$	I
5	DAD0	I	27	MODE	I
6	GND	–	28	GND	–
7	$\overline{CHG}$	O	29	$\overline{UDEN}$	O
8	DTO7	O	30	TSO5	O
9	DTO6	O	31	TSO4	O
10	DTO5	O	32	SDDO	O
11	DTO4	O	33	$\overline{DWN}$	O
12	GND	–	34	SUDI	I
13	DTO3	O	35	SUDO	O
14	DTO2	O	36	BCK	I
15	DTO1	O	37	$\overline{UP}$	O
16	DTO0	O	38	SDDI	I
17	V DD	–	39	V DD	–
18	DTI7	I	40	TSO3	O
19	DTI6	I	41	TSO2	O
20	DTI5	I	42	TSO1	O
21	DTI4	I	43	TSO0	O
22	DTI3	I	44	$\overline{CE}$	I

INPUT

BCK ; SERIAL DATA BIT CLOCK
$\overline{CE}$; PARALLEL DATA I/O ENABLE
DAD0-2 ; I/O DATA ADDRESS (DTI,DTO)
DTI0-7 ; PARALLEL DATA
MODE ; MODE CONTROL
(L ; CE, OE, WE, DAD0-2 / H ; DTO, DTI)
$\overline{OE}$; DTO OUTPUT ENABLE
$\overline{RST}$; RESET
SDDI ; MASTER UNIT SERIAL DATA
SUDI ; FOLLOWER UNIT SERIAL DATA
$\overline{WE}$; DTI WRITE ENABLE

OUTPUT

$\overline{CHG}$; FOLLOWER CHANGED DATA STATUS
(DD, CMD1, 2)
DTO0-7 ; PARALLEL DATA
$\overline{DWN}$; MASTER UNIT DATA BUS CONTROL
SDDO ; SERIAL DATA WITH CHANGED ADDRESS BIT
TO FOLLOWER UNIT
SUDO ; SERIAL DATA WITH ADDED UD TO MASTER UNIT
TSO0-5 ; TEST
$\overline{UDEN}$; UD SERIAL DATA ENABLE
$\overline{UP}$; FOLLOWER UNIT DATA BUS CONTROL


DAD0-2
5-3
CHG
7
DTO0-7
16-13
11-8
DTI0-7
25-18
CE
WE
OE
44
1
2
TIMING DEC
I/O TIMING
MUX
SYNC DATA REG
INIT DATA REG
UP REG
TEST MODE REG
DDCHG
DD
CD1CHG
CD1
CD2CHG
CD2
AD
Flag
CONTROL FLAG
27
MODE
DD REG & COMP
CMD1 REG & COMP
CMD2 REG & COMP
SYNC COMP
UD MUX
DEC
TEST MODE
SIPO
TEST OUTPUT SIGNALS
TEST MUX
43-40
31,30
TSO0-5
FRAME CNT & SYNC PROTECTION
PISO
SYOK
29
UDEN
37
UP
UDG
SDDI
38
ADOK
ADDRESS SET
TIMING GEN
33
DWN
SDDO
32
MUX
MUX
34
SUDI
BCK
36
35
SUDO
RST
26
ADG
CONTROL TIMING