IL22

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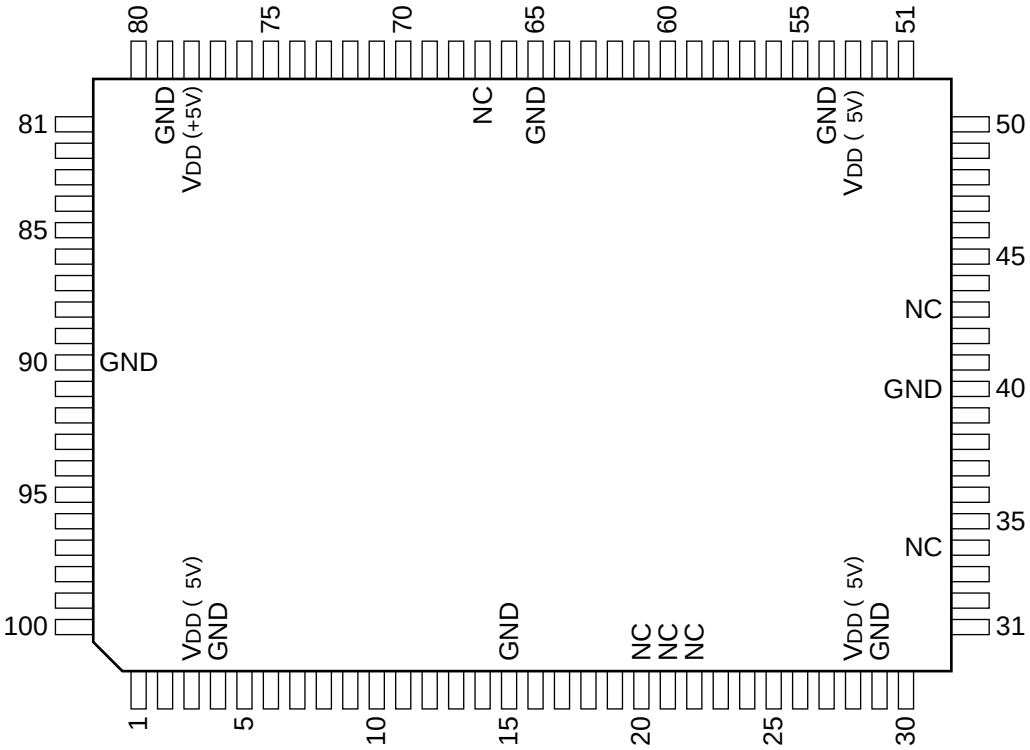
C-MOS SYNC GENERATOR

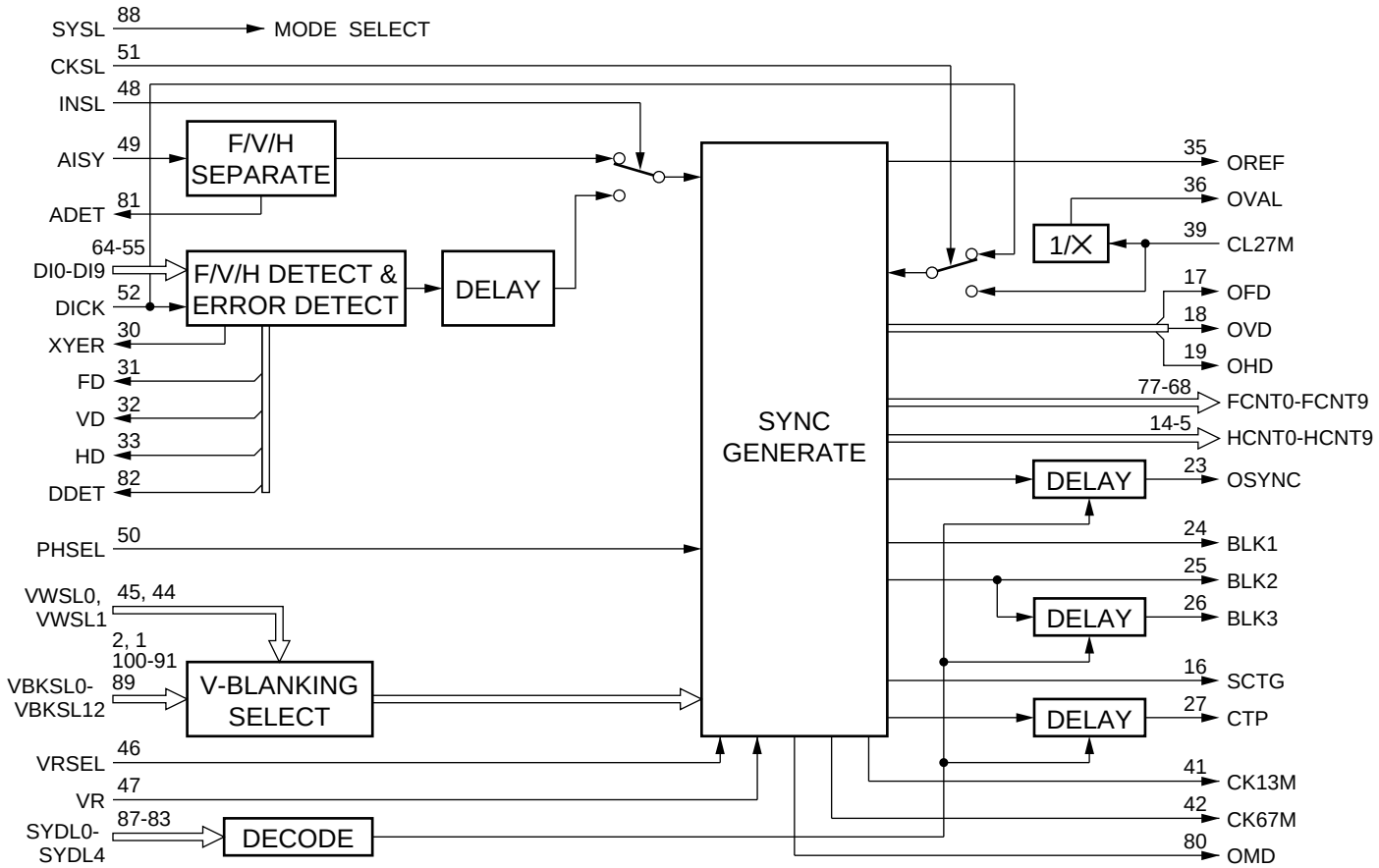
-TOP VIEW-



(V_{DD} = 5V)

PIN No.	I/O	SIGNAL	DESCRIPTION	PIN No.	I/O	SIGNAL	DESCRIPTION
1	I	VBKSL1	V-BLANKING LINE SELECT 1, 0	51	I	CKSL	CLOCK SELECT
2	I	VBKSL0		52	I	DICK	DIGITAL DATA CLOCK
3	—	V_{DD}		53	—	V_{DD}	
4	—	GND		54	—	GND	
5	O	HCNT9	H COUNTER 9-0	55	I	DI9	DATA9-0
6	O	HCNT8		56	I	DI8	
7	O	HCNT7		57	I	DI7	
8	O	HCNT6		58	I	DI6	
9	O	HCNT5		59	I	DI5	
10	O	HCNT4		60	I	DI4	
11	O	HCNT3		61	I	DI3	
12	O	HCNT2		62	I	DI2	
13	O	HCNT1		63	I	DI1	
14	O	HCNT0		64	I	DI0	
15	—	GND		65	—	GND	
16	O	SCTG	BURST GATE PULSE/BF	66	I	HALF	V-BLANKING SELECT(LAST LINE)
17	O	OFD	FIELD PULSE	67	—	NC	
18	O	OVD	V PULSE	68	O	FCNT9	LINE COUNTER 9-0
19	O	OHD	H PULSE	69	O	FCNT8	
20	—	NC		70	O	FCNT7	
21	—	NC		71	O	FCNT6	
22	—	NC		72	O	FCNT5	
23	O	OSYNC	COMPOSITE SYNC	73	O	FCNT4	
24	O	BLK1	BLANKING 1-3	74	O	FCNT3	
25	O	BLK2		75	O	FCNT2	
26	O	BLK3		76	O	FCNT1	
27	O	CTP	CLAMP PULSE/MASK	77	O	FCNT0	
28	—	V_{DD}		78	—	V_{DD}	
29	—	GND		79	—	GND	
30	O	XYER	XY-BYTE ERROR/PARITY CHECK	80	O	OMD	LINE MODE SELECT/DI0 LATCH
31	O	FD	FIELD PULSE/DI6 LATCH	81	O	ADET	ANALOG COMPOSITE SYNC DETECT
32	O	VD	V PULSE/DI5 LATCH	82	O	DDET	DIGITAL COMPONENT DATA DETECT
33	O	HD	H PULSE/DI4 LATCH	83	I	SYDL4	DELAY TIME SETTING 4-0
34	—	NC		84	I	SYDL3	
35	O	OREF	REF SIGNAL	85	I	SYDL2	
36	O	OVAL	VAL SIGNAL	86	I	SYDL1	
37	I	TST1	TEST 1, 2	87	I	SYDL0	
38	I	TST2		88	I	SYSL	SIGNAL SELECT
39	I	CL27M	VCXO OUT CLOCK 27 MHz/4fsc	89	I	VBKSL12	V-BLANKING LINE SELECT 12
40	—	GND		90	—	GND	
41	O	CK13M	13.5 MHz CLOCK/DI3 LATCH	91	I	VBKSL11	V-BLANKING LINE SELECT 11-2
42	O	CK67M	6.75 MHz CLOCK/DI1 LATCH	92	I	VBKSL10	
43	—	NC		93	I	VBKSL9	
44	I	VWSL1	V-BLANKING WIDTH SELECT 1, 0	94	I	VBKSL8	
45	I	VWSL0		95	I	VBKSL7	
46	I	VRSEL	VIDEO RESET SELECT	96	I	VBKSL6	
47	I	VR	VIDEO RESET	97	I	VBKSL5	
48	I	INSL	INPUT SELECT	98	I	VBKSL4	
49	I	AISY	ANALOG COMPOSITE SYNC	99	I	VBKSL3	
50	I	PHSEL	PHASE SELECT	100	I	VBKSL2	

422 MODE



4fsc MODE