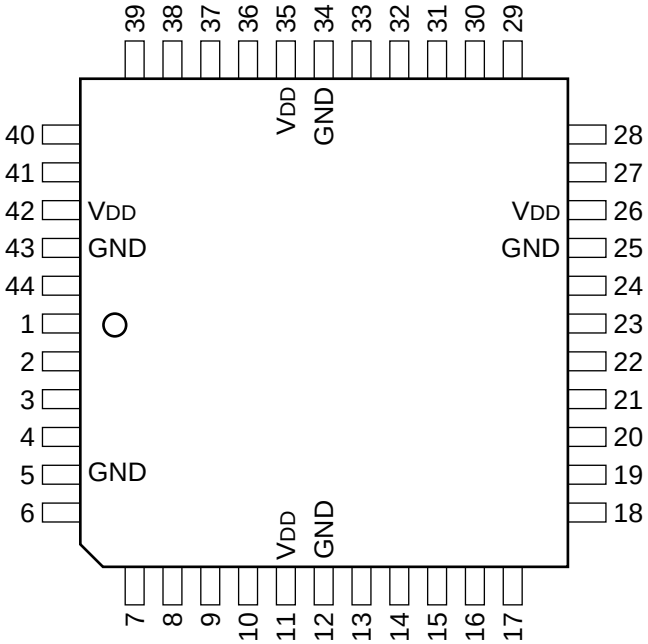
C-MOS HIPS

—TOP VIEW—



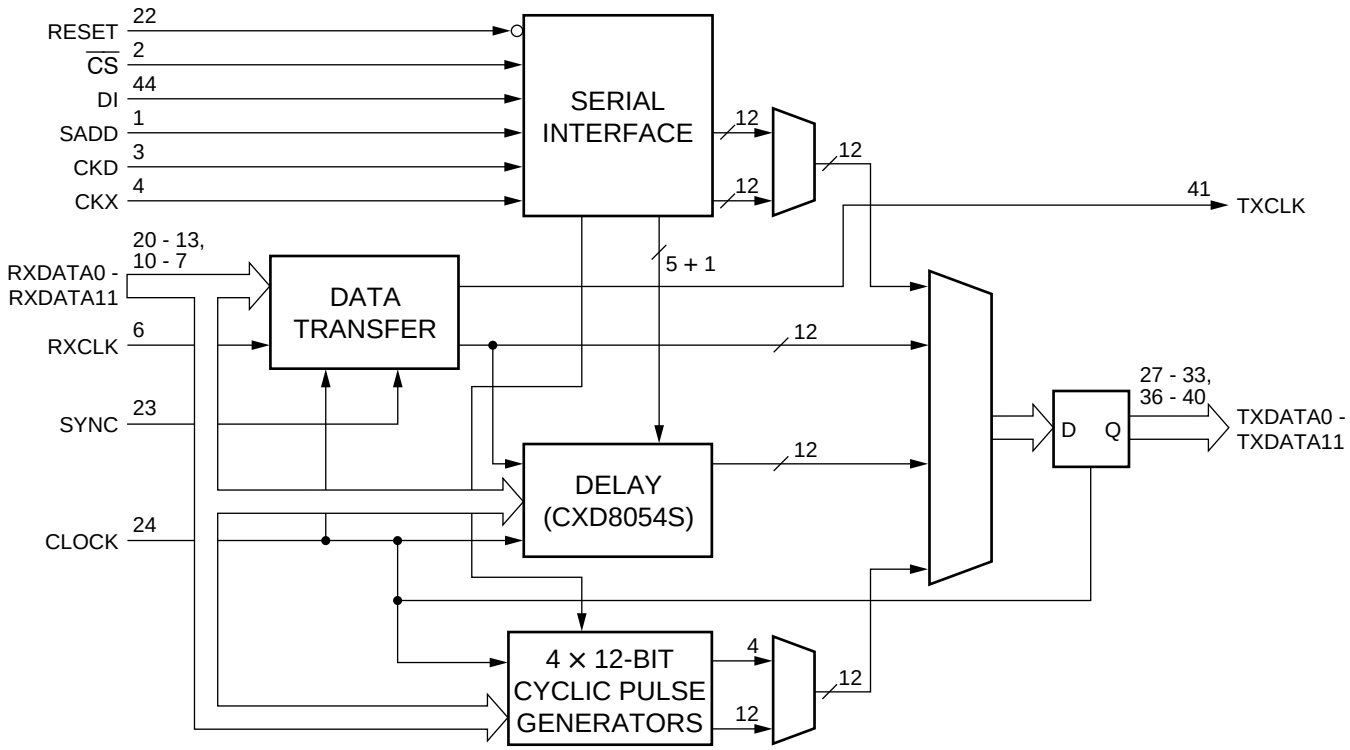
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	SADD	12	—	GND	23	I	SYNC	34	—	GND
2	I	$\overline{CS}$	13	I	RXDATA7	24	I	CLOCK	35	—	VDD
3	I	CKD	14	I	RXDATA6	25	—	GND	36	O	TXDATA7
4	I	CKX	15	I	RXDATA5	26	—	VDD	37	O	TXDATA8
5	—	GND	16	I	RXDATA4	27	O	TXDATA0	38	O	TXDATA9
6	I	RXCLK	17	I	RXDATA3	28	O	TXDATA1	39	O	TXDATA10
7	I	RXDATA11	18	I	RXDATA2	29	O	TXDATA2	40	O	TXDATA11
8	I	RXDATA10	19	I	RXDATA1	30	O	TXDATA3	41	O	TXCLK
9	I	RXDATA9	20	I	RXDATA0	31	O	TXDATA4	42	—	VDD
10	I	RXDATA8	21	O	PO	32	O	TXDATA5	43	—	GND
11	—	VDD	22	I	$\overline{RESET}$	33	O	TXDATA6	44	I	DI

INPUT

CKD	:	SERIAL INTERFACE DATA CLOCK
CKX	:	REGISTER ENABLE CLOCK
CLOCK	:	SYSTEM CLOCK
CS	:	CHIP SELECT FOR SERIAL INTERFACE, ACTIVE LOW
DI	:	SERIAL DATA INPUT
RESET	:	ASYNCHRONOUS RESET, ACTIVE LOW
RXCLK	:	RECEIVE CLOCK, 37.5 MHz
RXDATA0	:	DATA BIT 0/CYCLIC PULSE GENERATOR 1 LOAD
RXDATA1	:	DATA BIT 1/CYCLIC PULSE GENERATOR 1 ENABLE
RXDATA2	:	DATA BIT 2
RXDATA3	:	DATA BIT 3/CYCLIC PULSE GENERATOR 2 LOAD
RXDATA4	:	DATA BIT 4/CYCLIC PULSE GENERATOR 2 ENABLE
RXDATA5	:	DATA BIT 5
RXDATA6	:	DATA BIT 6/CYCLIC PULSE GENERATOR 3 LOAD
RXDATA7	:	DATA BIT 7/CYCLIC PULSE GENERATOR 3 ENABLE
RXDATA8	:	DATA BIT 8
RXDATA9	:	DATA BIT 9/CYCLIC PULSE GENERATOR 4 LOAD
RXDATA10	:	DATA BIT 10/CYCLIC PULSE GENERATOR 4 ENABLE
RXDATA11	:	DATA BIT 11
SADD	:	SERIAL ADDRESS BUS
SYNC	:	FRAME SYNC

OUTPUT

TXCLK	:	TRANSMIT CLOCK, 37.5 MHz
TXDATA0	:	OUTPUT DATA BIT 0
TXDATA1	:	OUTPUT DATA BIT 1
TXDATA2	:	OUTPUT DATA BIT 2/CYCLIC PULSE GENERATOR 1 PULSE
TXDATA3	:	OUTPUT DATA BIT 3
TXDATA4	:	OUTPUT DATA BIT 4
TXDATA5	:	OUTPUT DATA BIT 5/CYCLIC PULSE GENERATOR 2 PULSE
TXDATA6	:	OUTPUT DATA BIT 6
TXDATA7	:	OUTPUT DATA BIT 7
TXDATA8	:	OUTPUT DATA BIT 8/CYCLIC PULSE GENERATOR 3 PULSE
TXDATA9	:	OUTPUT DATA BIT 9
TXDATA10	:	OUTPUT DATA BIT 10
TXDATA11	:	OUTPUT DATA BIT 11/CYCLIC PULSE GENERATOR 4 PULSE
PO	:	PARAMETRIC OUTPUT FOR TEST, NOT CONNECTED


RESET
22
CS
2
DI
44
SADD
1
CKD
3
CKX
4
SERIAL INTERFACE
12
12
12
41
TXCLK
20 - 13, 10 - 7
RXDATA0 - RXDATA11
DATA TRANSFER
5 + 1
6
RXCLK
12
23
SYNC
27 - 33, 36 - 40
D
Q
TXDATA0 - TXDATA11
DELAY (CXD8054S)
12
24
CLOCK
4 × 12-BIT CYCLIC PULSE GENERATORS
4
12
12