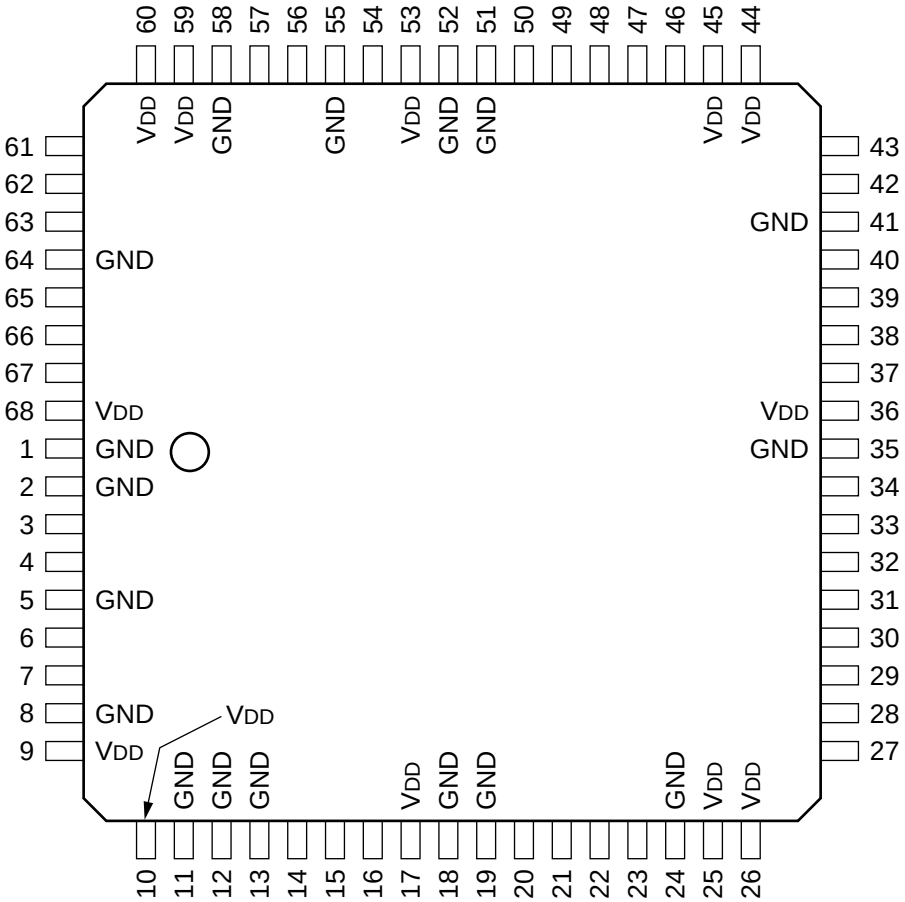
I/O PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	18	—	GND	35	—	GND	52	—	GND
2	—	GND	19	—	GND	36	—	V_{DD}	53	—	V_{DD}
3	O	DO6	20	O	TSTFM	37	I	DI2	54	I	FMCK
4	O	DO7	21	O	TSTH	38	I	DI1	55	—	GND
5	—	GND	22	O	TSTV	39	I	DI0	56	O	TSTOUT
6	O	DO8	23	I	$\overline{RSW}$	40	I	CKP	57	I	$\overline{OE}$
7	O	DO9	24	—	GND	41	—	GND	58	—	GND
8	—	GND	25	—	V_{DD}	42	I	CKX	59	—	V_{DD}
9	—	V_{DD}	26	—	V_{DD}	43	I	CKD	60	—	V_{DD}
10	—	V_{DD}	27	I	DI9	44	—	V_{DD}	61	O	DO0
11	—	GND	28	I	DI8	45	—	V_{DD}	62	O	DO1
12	—	GND	29	I	DI7	46	I	SMPL	63	O	DO2
13	—	GND	30	I	DI6	47	I	ADR	64	—	GND
14	I	TNEN	31	I	DI5	48	I	$\overline{CS}$	65	O	DO3
15	I	LTST	32	I	DI4	49	I/O	DIO	66	O	DO4
16	O	TSTERR	33	I	DI3	50	I	$\overline{RST}$	67	O	DO5
17	—	V_{DD}	34	I	CKI	51	—	GND	68	—	V_{DD}

INPUT

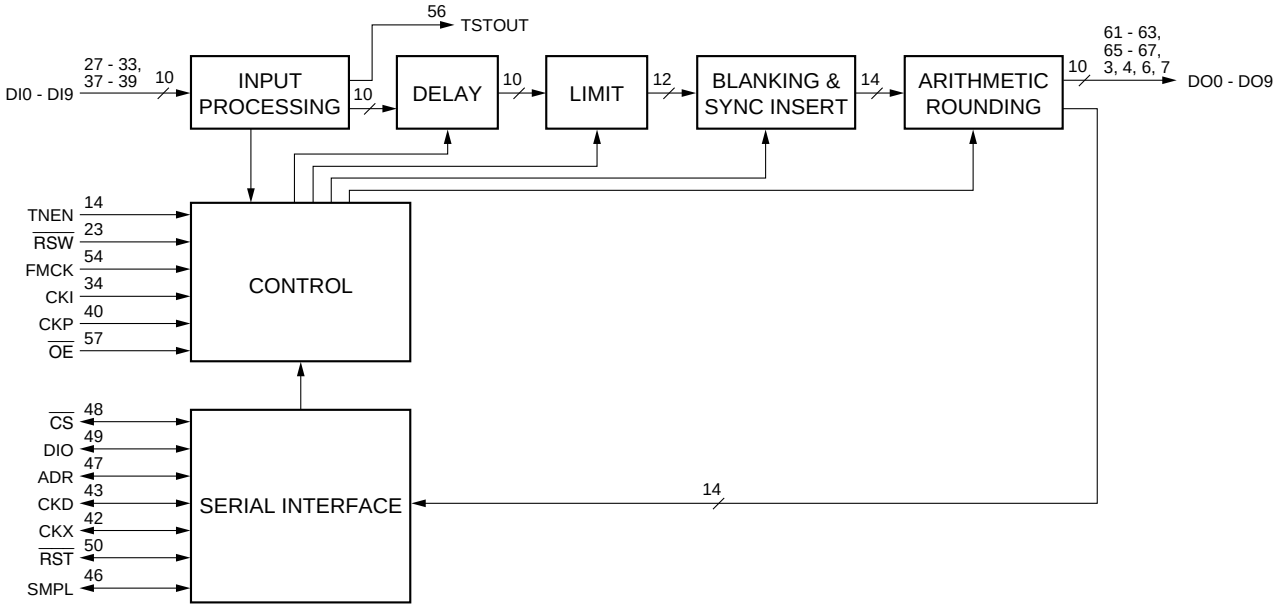
ADR : ADDRESS
CKD : CLOCK
CKI : 75 MHz TTL INPUT CLOCK
CKP : 75 MHz TTL OUTPUT CLOCK
CKX : LATCH UPDATE PULSE
$\overline{CS}$: CHIP SELECT
DI0 - DI9 : 10-BIT TTL VIDEO WITH DIGITAL SYNC
FMCK : FRAME CLOCK
LTST : LOAD TEST
$\overline{OE}$: DO BUS OUTPUT ENABLE
$\overline{RST}$: RESET
$\overline{RSW}$: FIFO RESET WRITE
SMPL : OUTPUT SMPLE
TNEN : PARAMETRIC TEST

OUTPUT

DO0 - DO9 : 10-BIT TTL VIDEO
TSTERR : SYNC ERROR FLAG
TSTFM : DELAYED FRAME RESET PULSE
TSTH : EXTRACTED HORIZONTAL SYNC
TSTOUT : PARAMETRIC TEST
TSTV : EXTRACTED VERTICAL (V/F) SYNC

INPUT/OUTPUT

DIO : BI-DIRECTIONAL DATA


56
TSTOUT
27 - 33,
37 - 39
DI0 - DI9
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INPUT
PROCESSING
10
DELAY
10
LIMIT
12
BLANKING &
SYNC INSERT
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61 - 63,
65 - 67,
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