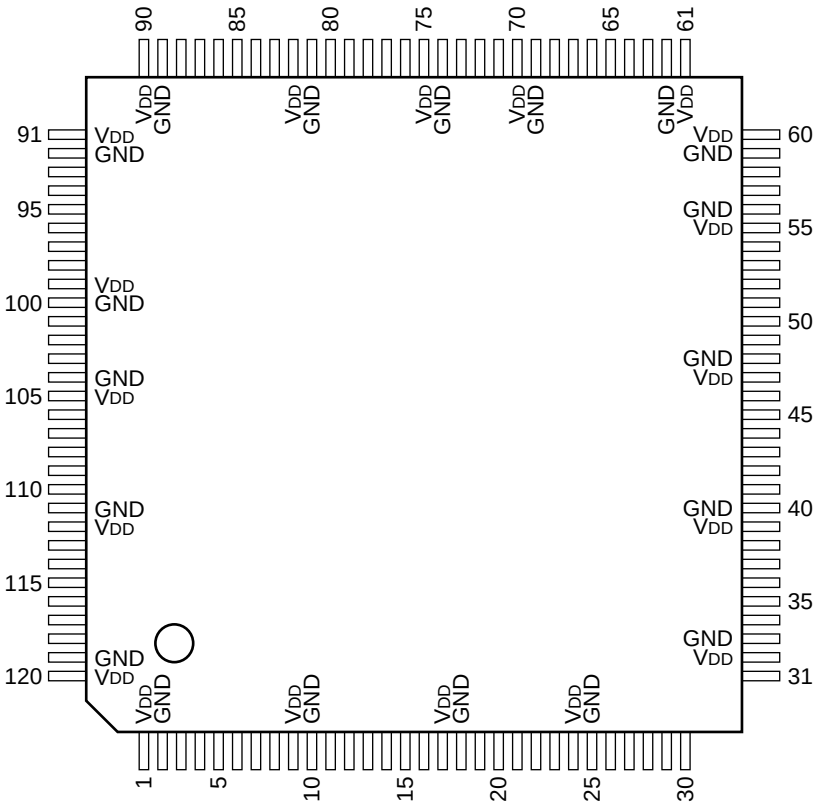
C-MOS KEY PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{DD}	31	—	V_{DD}	61	—	V_{DD}	91	—	V_{DD}
2	—	GND	32	—	GND	62	—	GND	92	—	GND
3	I	DIB16	33	I	DIA16	63	—	NC	93	—	NC
4	I	DIB15	34	I	DIA15	64	—	NC	94	I/O	DIO
5	I	DIB14	35	I	DIA14	65	—	NC	95	I	$\overline{CS}$
6	I	DIB13	36	I	DIA13	66	—	NC	96	I	ADR
7	I	DIB12	37	I	DIA12	67	—	NC	97	I	CKX
8	I	DIB11	38	I	DIA11	68	—	NC	98	I	CKD
9	—	V_{DD}	39	—	V_{DD}	69	—	GND	99	—	V_{DD}
10	—	GND	40	—	GND	70	—	V_{DD}	100	—	GND
11	I	DIB10	41	I	DIA10	71	O	DOX0	101	O	DOY0
12	I	DIB9	42	I	DIA9	72	O	DOX1	102	O	DOY1
13	I	DIB8	43	I	DIA8	73	O	DOX2	103	O	DOY2
14	I	DIB7	44	I	DIA7	74	—	GND	104	—	GND
15	I	DIB6	45	I	DIA6	75	—	V_{DD}	105	—	V_{DD}
16	I	DIB5	46	I	DIA5	76	O	DOX3	106	O	DOY3
17	—	V_{DD}	47	—	V_{DD}	77	O	DOX4	107	O	DOY4
18	—	GND	48	—	GND	78	O	DOX5	108	O	DOY5
19	I	DIB4	49	I	DIA4	79	O	DOX6	109	O	DOY6
20	I	DIB3	50	I	DIA3	80	O	DOX7	110	O	DOY7
21	I	DIB2	51	I	DIA2	81	—	GND	111	—	GND
22	I	DIB1	52	I	DIA1	82	—	V_{DD}	112	—	V_{DD}
23	I	DIB0	53	I	DIA0	83	O	DOX8	113	O	DOY8
24	—	V_{DD}	54	O	PO	84	O	DOX9	114	O	DOY9
25	—	GND	55	—	V_{DD}	85	O	DOX10	115	O	DOY10
26	—	NC	56	—	GND	86	O	DOX11	116	O	DOY11
27	—	NC	57	I	$\overline{RST}$	87	O	DOX12	117	O	DOY12
28	—	NC	58	I	CLK	88	I	$\overline{OEXL}$	118	I	$\overline{OEYL}$
29	—	NC	59	—	GND	89	—	GND	119	—	GND
30	—	NC	60	—	V_{DD}	90	—	V_{DD}	120	—	V_{DD}

INPUT

ADR	:	SERIAL ADDRESS
CKD	:	SERIAL INTERFACE CLOCK
CKX	:	SWITCHING TIMING PULSE
CLK	:	SYSTEM CLOCK
CS	:	CHIP SELECT
DIA0 - DIA16	:	CHANNEL-A 2’S COMPLEMENT DATA
DIB0 - DIB16	:	CHANNEL-B 2’S COMPLEMENT DATA
OEXL, OEYL	:	OUTPUT ENABLE
RST	:	SERIAL INTERFACE RESET

OUTPUT

DOX0 - DOX12	:	CHANNEL-X DATA
DOY0 - DOY12	:	CHANNEL-Y DATA
PO	:	PARAMETRIC OUTPUT FOR DEVICE TEST

INPUT/OUTPUT

DIO	:	SERIAL DATA