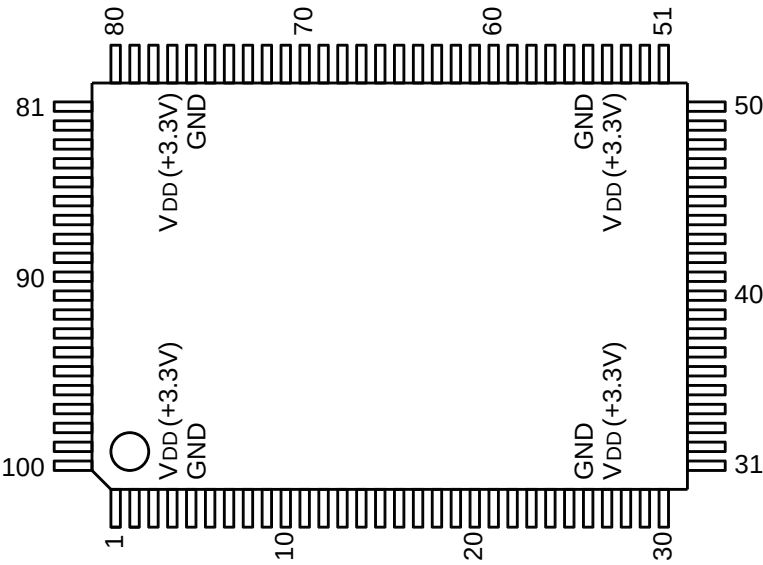

C-MOS DIGITAL FILTER
-TOP VIEW-



(V_{DD} = +3.3V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	EI5	21	I	SI1	41	I	CS	61	O	SO4	81	O	DO6
2	I	EI4	22	I	SI0	42	I	OB2S	62	O	SO5	82	O	DO7
3	I	EI3	23	I	RND	43	O	EO0	63	O	SO6	83	O	DO8
4	–	V _{DD}	24	I	DI11	44	O	EO1	64	O	SO7	84	O	DO9
5	–	GND	25	I	DI10	45	O	EO2	65	O	SO8	85	O	DO10
6	I	EI2	26	–	GND	46	O	EO3	66	O	SO9	86	O	DO11
7	I	EI1	27	–	V _{DD}	47	O	EO4	67	O	SO10	87	O	PO
8	I	EI0	28	I	DI9	48	O	EO5	68	O	SO11	88	O	CKXO
9	I	SI13	29	I	DI8	49	O	EO6	69	O	SO12	89	I	MOD1
10	I	SI12	30	I	DI7	50	O	EO7	70	O	SO13	90	I	MOD0
11	I	SI11	31	I	DI6	51	O	EO8	71	O	DO0	91	I	HD
12	I	SI10	32	I	DI5	52	O	EO9	72	O	DO1	92	I	MYS
13	I	SI9	33	I	DI4	53	O	EO10	73	O	DO2	93	I	LM1
14	I	SI8	34	I	DI3	54	–	V _{DD}	74	O	DO3	94	I	LM0
15	I	SI7	35	I	DI2	55	–	GND	75	O	DO4	95	I	EI11
16	I	SI6	36	I	DI1	56	O	EO11	76	–	GND	96	I	EI10
17	I	SI5	37	I	DI0	57	O	SO0	77	–	V _{DD}	97	I	EI9
18	I	SI4	38	I	CKXI	58	O	SO1	78	I	OE	98	I	EI8
19	I	SI3	39	I	DATA	59	O	SO2	79	I	CK	99	I	EI7
20	I	SI2	40	I	CKD	60	O	SO3	80	O	DO5	100	I	EI6

23	RND				
24	DI11	DO11	86		
25	DI10	DO10	85		
28	DI9	DO9	84		
29	DI8	DO8	83		
30	DI7	DO7	82	INPUT	
31	DI6	DO6	81	CK	; DEVICE CLOCK (MAX 28.6MHz)
32	DI5	DO5	80	CKD	; SERIAL INTERFACE DATA CLOCK
33	DI4	DO4	75	CKXI	; SERIAL INTERFACE LATCH CLOCK
34	DI3	DO3	74	$\overline{CS}$	; SERIAL INTERFACE CHIP SELECT
35	DI2	DO2	73	DATA	; SERIAL INTERFACE DATA
36	DI1	DO1	72	DI (0-11)	; DATA INPUTS
37	DI0	DO0	71	EI (0-11)	; EXPANSION DATA INPUT
				HD	; MULTIPLEX TIMING CONTROL
95	EI11	EO11	56	LM (0,1)	; LIMITER CONTROL
96	EI10	EO10	53		
97	EI9	EO9	52		
98	EI8	EO8	51		
99	EI7	EO7	50		
100	EI6	EO6	49		
1	EI5	EO5	48		
2	EI4	EO4	47	MOD0	; MODE CONTROL (TAP)
3	EI3	EO3	46		
6	EI2	EO2	45		
7	EI1	EO1	44		
8	EI0	EO0	43	MOD1	; MODE CONTROL (CASCADE)
9	SI13	SO13	70		
10	SI12	SO12	69		
11	SI11	SO11	68		
12	SI10	SO10	67	MYS	; EMULATION (H ; CXD8055 EMULATION L ; NORMAL)
13	SI9	SO9	66		
14	SI8	SO8	65	OB2S	; NUMBER FORMAT (H ; 2'S COMPLEMENT L ; OFFSET BINARY)
15	SI7	SO7	64	$\overline{OE}$	; OUTPUT ENABLE
16	SI6	SO6	63	RND	; PARTIAL SUM RUNDING BIT
17	SI5	SO5	62	SI (0-13)	; FILTER PARTIAL INPUT
18	SI4	SO4	61		
19	SI3	SO3	60		
20	SI2	SO2	59	OUTPUT	
21	SI1	SO1	58	CKXO	; LATCH CLOCK OUTPUT
22	SI0	SO0	57	DO (0-11)	; CASCADE DATA OUTPUT
				EO (0-11)	; EXPANSION DATA OUTPUT
93	LM1	OE	78	PO	; PARAMETRIC OUTPUT (TEST ONLY)
94	LM0			SO (0-13)	; FILTER OUTPUT
89	MOD1	MYS	92		
90	MOD0				
42	OB2S	PO	87		
38	CKXI	CKXO	88		
39	DATA				
40	CKD				
41	CS				

LM1	LM0	SO OUTPUT
0	0	11 BIT
0	1	12 BIT
1	0	13 BIT
1	1	14 BIT

0 ; LOW LEVEL
1 ; HIGH LEVEL

MODE0	FUNCTION MODE
0	ZERO INSERTED
1	NORMAL TAP

0 ; LOW LEVEL
1 ; HIGH LEVEL

MODE1	FUNCTION MODE
0	PARTIAL TAP DEVICE
1	CENTER TAP DEVICE

0 ; LOW LEVEL
1 ; HIGH LEVEL

