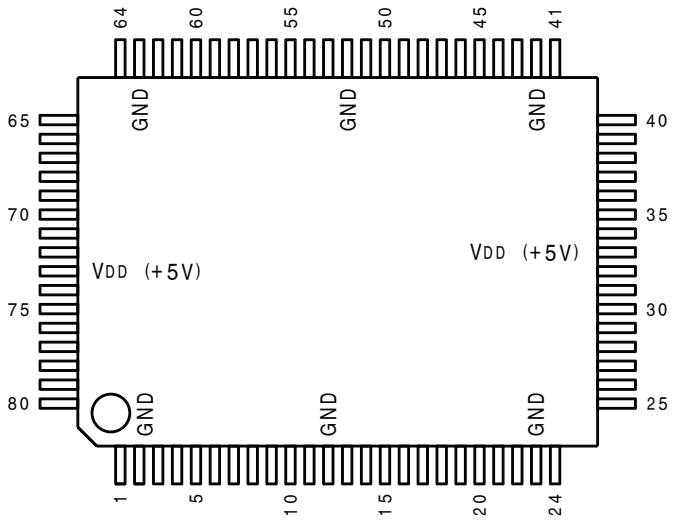
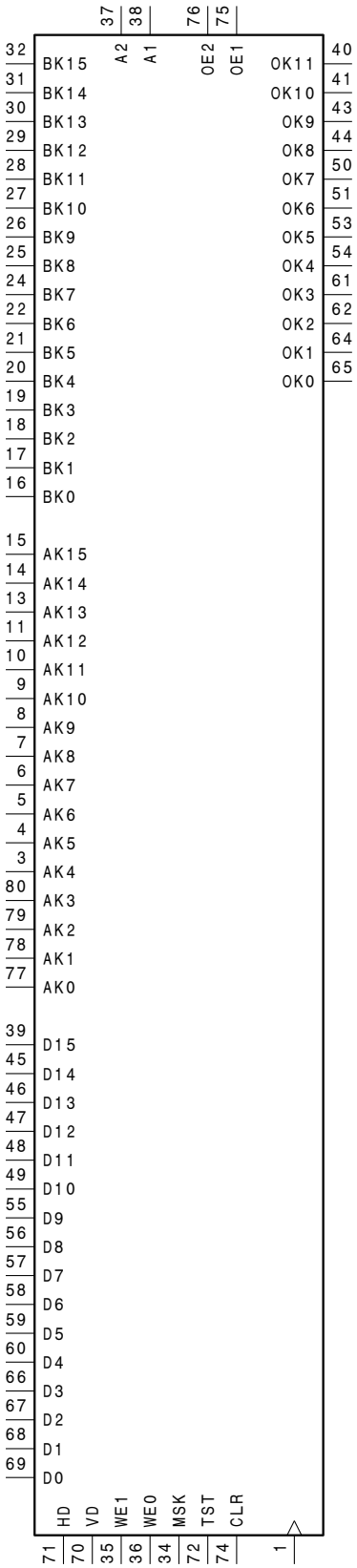
KEY SIGNAL PROCESSOR

-TOP VIEW-



(V DD=+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	CLK	21	I	BK5	41	O	OK10	61	O	OK3
2	–	GND	22	I	BK6	42	–	GND	62	O	OK2
3	I	AK4	23	–	GND	43	O	OK9	63	–	GND
4	I	AK5	24	I	BK7	44	O	OK8	64	O	OK1
5	I	AK6	25	I	BK8	45	I	D14	65	O	OK0
6	I	AK7	26	I	BK9	46	I	D13	66	I	D3
7	I	AK8	27	I	BK10	47	I	D12	67	I	D2
8	I	AK9	28	I	BK11	48	I	D11	68	I	D1
9	I	AK10	29	I	BK12	49	I	D10	69	I	D0
10	I	AK11	30	I	BK13	50	O	OK7	70	I	VD
11	I	AK12	31	I	BK14	51	O	OK6	71	I	HD
12	–	GND	32	I	BK15	52	–	GND	72	I	TST
13	I	AK13	33	–	VDD	53	O	OK5	73	–	VDD
14	I	AK14	34	I	MSK	54	O	OK4	74	I	CLR
15	I	AK15	35	I	WE1	55	I	D9	75	I	OE1
16	I	BK0	36	I	WE0	56	I	D8	76	I	OE2
17	I	BK1	37	I	A2	57	I	D7	77	I	AK0
18	I	BK2	38	I	A1	58	I	D6	78	I	AK1
19	I	BK3	39	I	D15	59	I	D5	79	I	AK2
20	I	BK4	40	O	OK11	60	I	D4	80	I	AK3

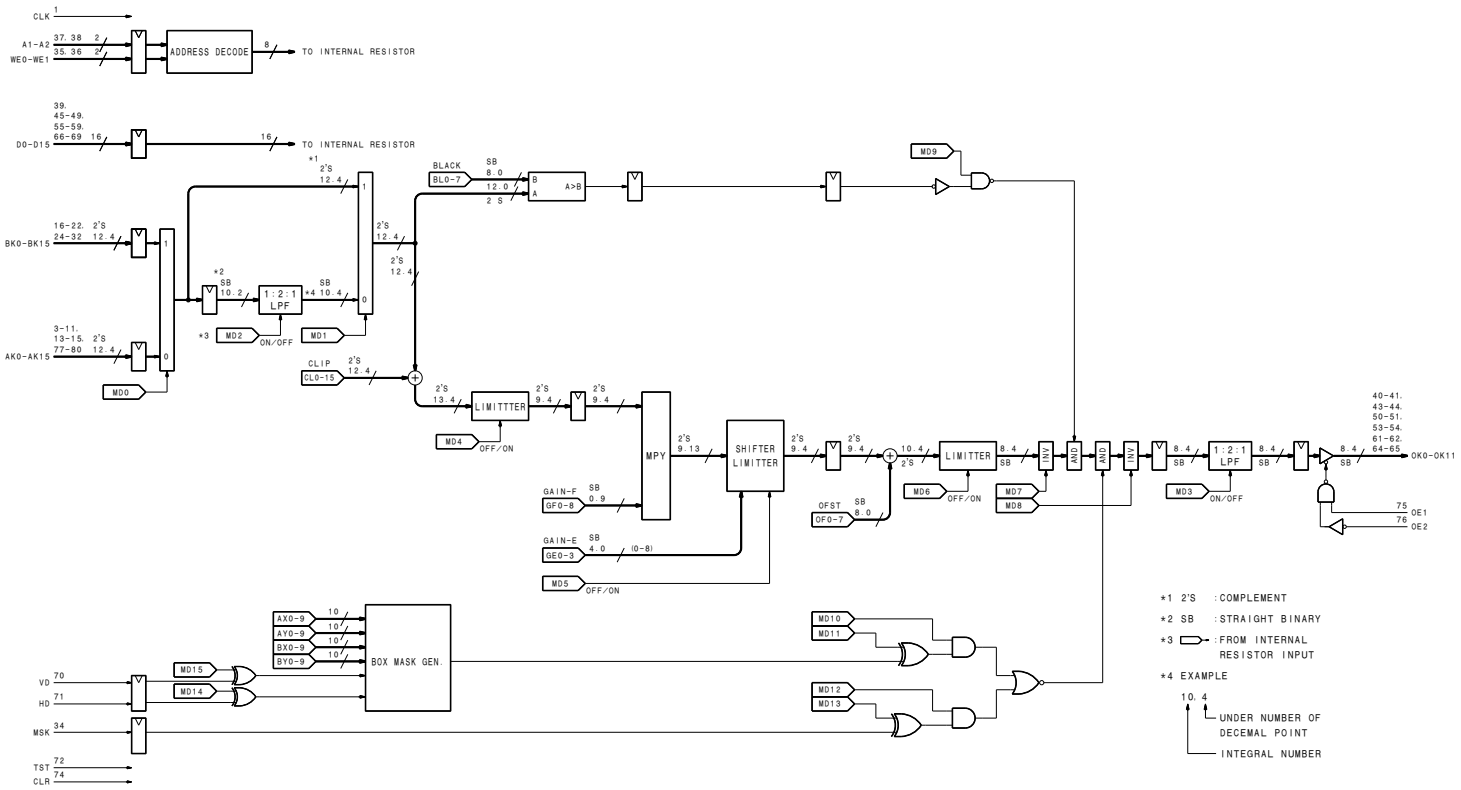


INPUT

A1	;ADDRESS 2EXP0
A2	;ADDRESS 2EXP1
AK0-AK15	;AK DATA (16 BIT)
BK0-BK15	;BK DATA (16 BIT)
CLK	;CLOCK
CLR	;CLEAR
D0-D15	;DATA (16 BIT)
HD	;HD SIGNAL
MSK	;EXTERNAL MASK
OE1	;OUTPUT ENABLE (+)
OE2	;OUTPUT ENABLE (-)
TST	;TEST TERMINAL
VD	;VD SIGNAL
WE0	;WRITE ENABLE 0
WE1	;WRITE ENABLE 1

OUTPUT

OK0-OK11	;KEY SIGNAL OUTPUT (12 BIT)


CLK
A1-A2
WE0-WE1
ADDRESS DECODE
TO INTERNAL RESISTOR
D0-D15
TO INTERNAL RESISTOR
BK0-BK15
AK0-AK15
MD0
MD1
MD2
ON/OFF
1:2:1 LPF
CLIP
CL0-15
BLACK
BL0-7
A>B
MD4
OFF/ON
LIMITTER
MPY
SHIFTER LIMITTER
GAIN-F
GF0-8
GAIN-E
GE0-3
MD5
OFST
OF0-7
MD6
MD7
MD8
MD3
MD9
INV
AND
OK0-OK11
OE1
OE2
AX0-9
AY0-9
BX0-9
BY0-9
BOX MASK GEN.
MD15
MD14
VD
HD
MSK
TST
CLR
MD10
MD11
MD12
MD13
*1 2'S : COMPLEMENT
*2 SB : STRAIGHT BINARY
*3 : FROM INTERNAL RESISTOR INPUT
*4 EXAMPLE
10.4
UNDER NUMBER OF DECEMAL POINT
INTEGRAL NUMBER