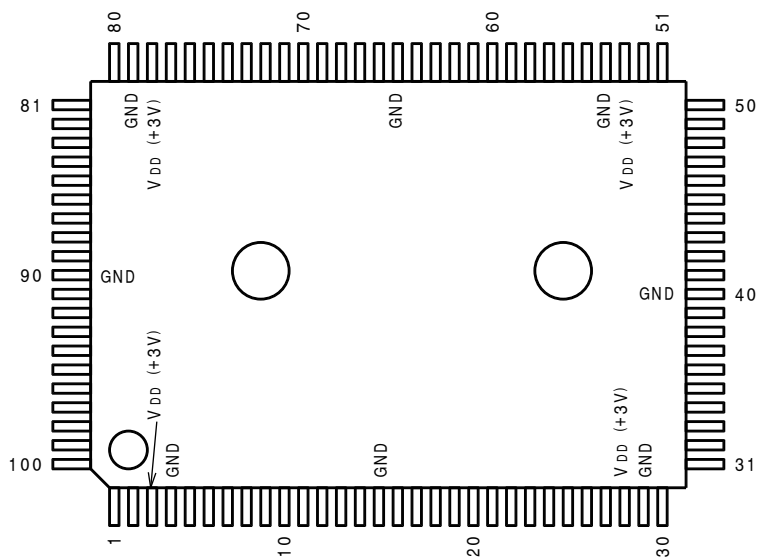


C-MOS FINE KEY PROCESSOR

-TOP VIEW-

(V_{DD} = +3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	KI3402	21	I/O	CM17	41	O	CS011	61	I	CKX	81	I	KI07
2	I	KI3403	22	I/O	CM18	42	O	CS010	62	I	ADD	82	I	KI08
3	-	V _{DD}	23	I/O	CM19	43	O	CS09	63	I	CKD	83	I	KI09
4	-	GND	24	I/O	CM110	44	O	CS08	64	I	$\overline{\text{RST}}$	84	I	KI010
5	I	KI3404	25	I/O	CM111	45	O	CS07	65	-	GND	85	I	KI011
6	I	KI3405	26	O	CM011	46	O	CS06	66	I/O	DIO	86	I	KI120
7	I	KI3406	27	O	CM010	47	O	CS05	67	I	XTS0	87	I	KI121
8	I	KI3407	28	-	V _{DD}	48	O	CS04	68	I	XTS1	88	I	KI122
9	I	KI3408	29	-	GND	49	O	CS03	69	I	XTS2	89	I	KI123
10	I	KI3409	30	O	CM09	50	O	CS02	70	I	XTS3	90	-	GND
11	I	KI3410	31	O	CM08	51	O	CS01	71	I	XTS4	91	I	KI124
12	I	KI3411	32	O	CM07	52	I	CK	72	I	KI00	92	I	KI125
13	I/O	CM10	33	O	CM06	53	-	V _{DD}	73	I	KI01	93	I	KI126
14	I/O	CM11	34	O	CM05	54	-	GND	74	I	KI02	94	I	KI127
15	-	GND	35	O	CM04	55	O	CS00	75	I	KI03	95	I	KI128
16	I/O	CM12	36	O	CM03	56	I	$\overline{\text{CS1}}$	76	I	KI04	96	I	KI129
17	I/O	CM13	37	O	CM02	57	I	$\overline{\text{CS2}}$	77	I	KI05	97	I	KI1210
18	I/O	CM14	38	O	CM01	58	I	XSMP	78	-	V _{DD}	98	I	KI1211
19	I/O	CM15	39	O	CM00	59	I	XMM	79	-	GND	99	I	KI340
20	I/O	CM16	40	-	GND	60	I	HD	80	I	KI06	100	I	KI341

85	KI0 11	CS0 11	41
84	KI0 10	CS0 10	42
83	KI0 9	CS0 9	43
82	KI0 8	CS0 8	44
81	KI0 7	CS0 7	45
80	KI0 6	CS0 6	46
77	KI0 5	CS0 5	47
76	KI0 4	CS0 4	48
75	KI0 3	CS0 3	49
74	KI0 2	CS0 2	50
73	KI0 1	CS0 1	51
72	KI0 0	CS0 0	55
98	KI12 11	CMO 11	26
97	KI12 10	CMO 10	27
96	KI12 9	CMO 9	30
95	KI12 8	CMO 8	31
94	KI12 7	CMO 7	32
93	KI12 6	CMO 6	33
92	KI12 5	CMO 5	34
91	KI12 4	CMO 4	35
89	KI12 3	CMO 3	36
88	KI12 2	CMO 2	37
87	KI12 1	CMO 1	38
86	KI12 0	CMO 0	39
12	KI34 11	HD	60
11	KI34 10		52
10	KI34 9		
9	KI34 8	CS1	56
8	KI34 7	CS2	57
7	KI34 6	SMPL	58
6	KI34 5	ADD	62
5	KI34 4	DIO	66
2	KI34 3	CKD	63
1	KI34 2	CKX	61
100	KI34 1	RST	64
99	KI34 0		
		XMM	59
25	CMI 11	XTS4	71
24	CMI 10	XTS3	70
23	CMI 9	XTS2	69
22	CMI 8	XTS1	68
21	CMI 7	XTS0	67
20	CMI 6		
19	CMI 5		
18	CMI 4		
17	CMI 3		
16	CMI 2		
14	CMI 1		
13	CMI 0		

INPUT

ADD ; ADDRESS FOR SERIAL CONTROL
 CK ; MAIN CLOCK
 CKD ; CLOCK FOR SERIAL CONTROL
 CKX ; SWITCHING TIMING PULSE
 CS 1, 2 ; CHIP SELECT FOR SERIAL CONTROL
 HD ; H DRIVE
 KI0 (0-11) ; KEY SIGNAL
 (KEYZ/KEY0 MULTIPLEXED)
 *KEY0 - KEY SIGNAL (0 LINE DELAYED)
 KI12 (0-11) ; KEY SIGNAL
 (KEY1/KEY2 MULTIPLEXED)
 *KEY1 - KEY SIGNAL (1 LINE DELAYED)
 *KEY2 - KEY SIGNAL (2 LINE DELAYED)
 KI34 (0-11) ; KEY SIGNAL
 (KEY3/KEY4 MULTIPLEXED)
 *KEY3 - KEY SIGNAL (3 LINE DELAYED)
 *KEY4 - KEY SIGNAL (4 LINE DELAYED)
 RST ; RESET FOR CHIP
 SMPL ; SAMPLE PULSE
 XMM ; TEST FOR MULTIPLIER CHECK
 XTS (0-4) ; TEST MODE CONTROL

OUTPUT

CMO (0-11) ; COMBINER (MAIN OUTPUT)
 CSO (0-11) ; CASCADE

INPUT/OUTPUT

CMI (0-11) ; COMBINER
 DIO ; SERIAL CONTROL DATA

