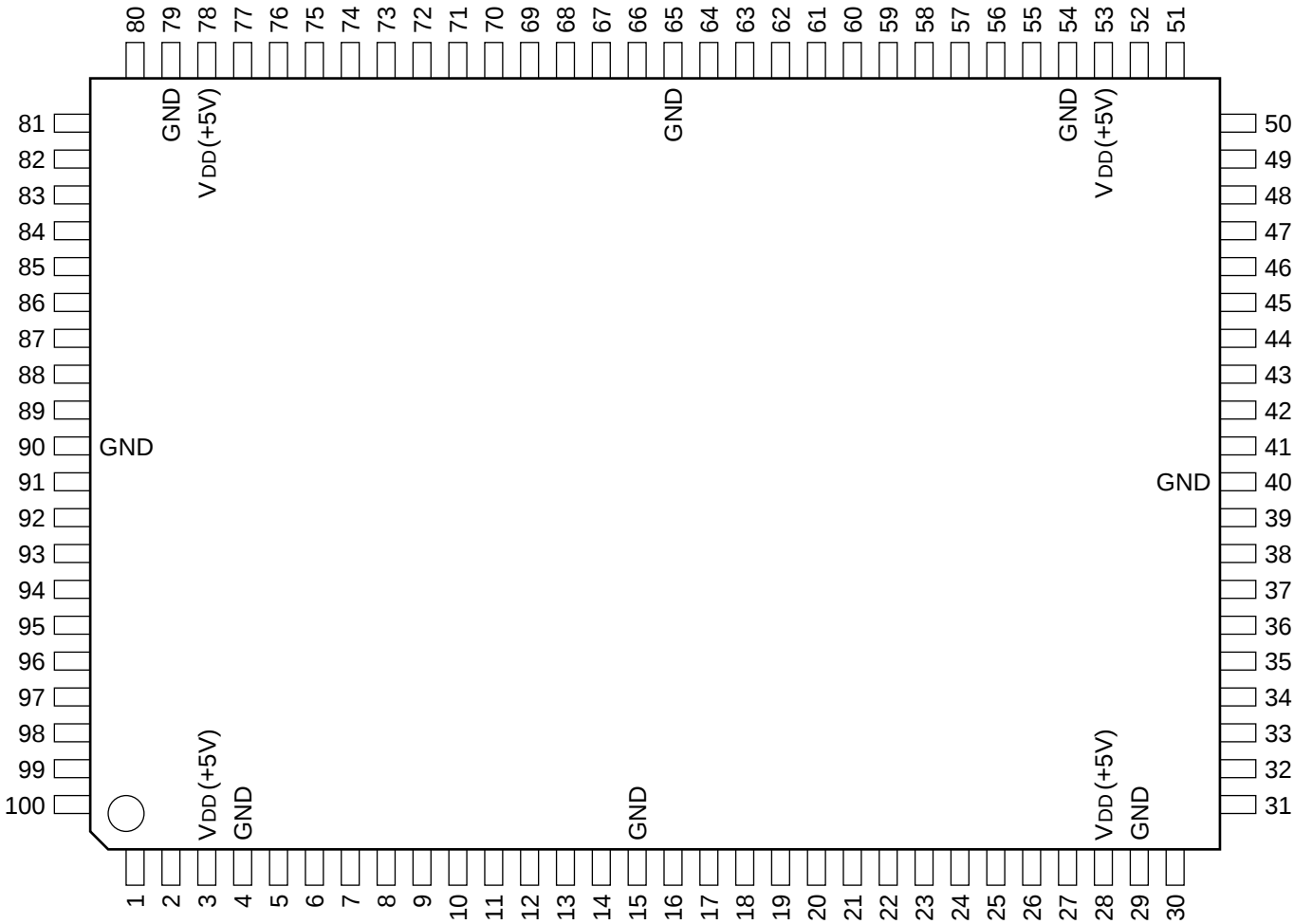

C-MOS MEMORY CONTROLLER FOR FRAME SYNCHRONIZER
- TOP VIEW -



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	OY2	26	I/O	IU2/OU2	51	I	D3	76	O	BEN1O
2	O	OY3	27	I/O	IU3/OU3	52	I	D2	77	O	BEN1E
3	–	V _{DD}	28	–	V _{DD}	53	–	V _{DD}	78	–	V _{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	O	OY4	30	I/O	IU4/OU4	55	I	D1	80	O	AEN1O
6	O	OY5	31	I/O	IU5/OU5	56	I	D0	81	O	AEN1E
7	O	OY6	32	I/O	IU6/OU6	57	I	HD	82	O	INC1
8	O	OY7	33	I/O	IU7/OU7	58	I	VD	83	O	HCLR1
9	I	YDL2	34	I	IV4/IC4	59	I	FLD	84	O	VCLR1
10	I	YDL3	35	I	IV5/IC5	60	O	OLD2	85	I	BLK
11	O	OC0/OV0	36	I	IV6/IC6	61	O	AUX2	86	I	KS
12	O	OC1/OV1	37	I	IV7/IC7	62	O	INH2	87	I	IK
13	O	OC2/OV2	38	I	PS	63	O	BEN2O	88	I	IY0
14	O	OC3/OV3	39	I	MOD	64	O	BEN2E	89	I	IY1
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	OC4/OV4	41	I	CK	66	O	AEN2O	91	I	IY2
17	O	OC5/OV5	42	I	ILD	67	O	AEN2E	92	I	IY3
18	O	OC6/OV6	43	I	WE2	68	O	INC2	93	I	IY4
19	O	OC7/OV7	44	I	WE1	69	O	HCLR2	94	I	IY5
20	I	IV0/IC0	45	I	A1	70	O	VCLR2	95	I	IY6
21	I	IV1/IC1	46	I	A0	71	I	TST	96	I	IY7
22	I	IV2/IC2	47	I	D7	72	I	CLR	97	I	YDL0
23	I	IV3/IC3	48	I	D6	73	O	OLD1	98	I	YDL1
24	I/O	IU0/OU0	49	I	D5	74	O	AUX1	99	O	OY0
25	I/O	IU1/OU1	50	I	D4	75	O	INH1	100	O	OY1

56	D0	VCLR1	84	INPUT	
55	D1	HCLR1	83	A0, A1	; ADDRESS BUS
52	D2	INC1	82	BLK	; BLANKING
51	D3	AEN1E	81	CK	; CLOCK
50	D4	AEN1O	80	CLR	; CLEAR
49	D5	BEN1E	77	D0-D7	; DATA BUS
48	D6	BEN1O	76	FLD	; FIELD (L ; EVEN, H ; ODD)
47	D7	INH1	75	HD	; HORIZONTAL SYNCHRONIZED
		AUX1	74	IK	; 1 BIT KEY
46	A0	OLD1	73	ILD	; LOAD
45	A1			IV0/IC0-IV7/IC7	; PARALLEL DATA INPUT OF V DATA AT PARALLEL-SERIAL MODE, SERIAL DATA INPUT OF UV DATA AT SERIAL-PARALLEL MODE.
		VCLR2	70		
44	WE1	HCLR2	69	IY0-IY7	; Y DATA BUS
43	WE2	INC2	68	KS	; KEY SELECT
		AEN2E	67	MOD	; MODE SELECT (L ; 4:1:1 MODE, H : 4:2:2 MODE)
72	CLR	AEN2O	66	PS	; PARALLEL-SERIAL / SERIAL-PARALLEL SELECT (L ; S → P, H ; P → S)
		BEN2E	64	TST	; TEST
57	HD	BEN2O	63	VD	; VERTICAL SYNCHRONIZED
58	VD	INH2	62	WE1, WE2	; WRITE ENABLE
59	FLD	AUX2	61	YDL0-YDL3	; Y DATA DELAY
71	TST	OLD2	60		
				OUTPUT	
41	>			AEN1E, AEN2E	; A CH EVEN FIELD ENABLE
				BEN1E, BEN2E	; B CH EVEN FIELD ENABLE
88	IY0	OY0	99	AEN1O, AEN2O	; A CH ODD FIELD ENABLE
89	IY1	OY1	100	BEN1O, BEN2O	; B CH ODD FIELD ENABLE
91	IY2	OY2	1	AUX1, AUX2	; MODE 0,1 ; MSB (AUX BIT) OUTPUT OF MD 1-2 REGISTER.
92	IY3	OY3	2		MODE 2 ; HIGH BIT OUTPUT OF LOAD COUNTER.
93	IY4	OY4	5		MODE 3 ; H LEVEL OUTPUT OF LINE NUMBER SET AT VC1-2
94	IY5	OY5	6		REGISTER EVERY V RESET.
95	IY6	OY6	7		H LEVEL OUTPUT AT ALL TIMES WHEN VC1-2=0.
96	IY7	OY7	8	HCLR1, HCLR2	; HORIZONTAL CLEAR
				INC1, INC2	; LINE INCREMENT
97	YDL0			INH1, INH2	; INHIBIT
98	YDL1			OC0/OV0-OC7/OV7	; SERIAL DATA OUTPUT OF UV DATA AT PARALLEL-SERIAL MODE, PARALLEL DATA OUTPUT OF V DATA AT SERIAL-PARALLEL MODE.
9	YDL2				
10	YDL3			OLD1, OLD2	; MODE 0 ; L LEVEL WHEN LOAD COUNTER OUTPUT IS 0 AT LOAD SIGNAL FOR 4:1:1 MODE OF UV DATA CONVERTER.
		IU0/OU0	24		
87	IK	IU1/OU1	25		MODE 1,2 ; LOW BIT OUTPUT OF LOAD COUNTER AT LOAD SIGNAL
86	KS	IU2/OU2	26		FOR 4:2:2 MODE OF UV DATA CONVERTER.
		IU3/OU3	27		MODE 3 ; H LEVEL OUTPUT OF CLOCK NUMBER SET AT LD1-2
20	IV0/IC0	IU4/OU4	30		REGISTER EVERY H RESET.
21	IV1/IC1	IU5/OU5	31		H LEVEL OUTPUT AT ALL TIMES WHEN LD1-2=0.
22	IV2/IC2	IU6/OU6	32		H LEVEL OUTPUT WHEN AUX1-2 (MODE 3) IS H LEVEL.
23	IV3/IC3	IU7/OU7	33	OY0-OY7	; Y DATA BUS
34	IV4/IC4			VCLR1, VCLR2	; VERTICAL CLEAR
35	IV5/IC5	OC0/OV0	11		
36	IV6/IC6	OC1/OV1	12	INPUT/OUTPUT	
37	IV7/IC7	OC2/OV2	13	IU0/OU0-IU7/OU7	; SERIAL DATA OUTPUT OF U DATA AT PARALLEL-SERIAL MODE, PARALLEL DATA OUTPUT OF U DATA AT SERIAL-PARALLEL MODE.
		OC3/OV3	14		
42	ILD	OC4/OV4	16		
39	MOD	OC5/OV5	17		
38	PS	OC6/OV6	18		
85	BLK	OC7/OV7	19		

