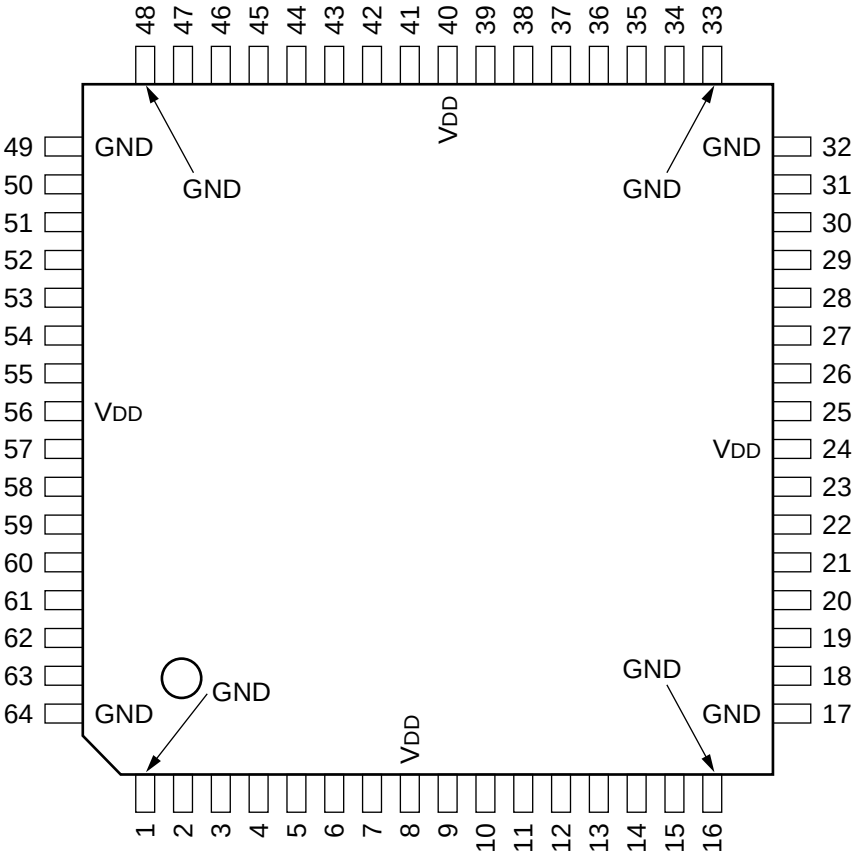
C-MOS VARIABLE DELAY CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	17	—	GND	33	—	GND	49	—	GND
2	I	D14	18	I	D1	34	O	Q2	50	O	Q15
3	I	D13	19	I	D0	35	O	Q3	51	I	C0
4	I	D12	20	I	CLR*	36	O	Q4	52	I	C1
5	I	D11	21	I	G	37	O	Q5	53	I	C2
6	I	D10	22	I	M0	38	O	Q6	54	I	C3
7	I	D9	23	I	M1	39	O	Q7	55	I	C4
8	—	VDD	24	—	VDD	40	—	VDD	56	—	VDD
9	I	D8	25	I	M2	41	O	Q8	57	I	C5
10	I	D7	26	O	TSTO	42	O	Q9	58	I	C6
11	I	D6	27	I	RST	43	O	Q10	59	I	C7
12	I	D5	28	I	CK	44	O	Q11	60	I	C8
13	I	D4	29	I	$\overline{OE}$	45	O	Q12	61	I	C9
14	I	D3	30	O	Q0	46	O	Q13	62	I	C10
15	I	D2	31	O	Q1	47	O	Q14	63	I	D15
16	—	GND	32	—	GND	48	—	GND	64	—	GND

*20 PIN

CXD8875AR	CLR
CXD8875R	INV

INPUT

C10 - C0 : DELAY DIRECT CONTROL

TERMINAL											DELAY TIME (CK)		
C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	LONG	DOUBLE	WIDE
0	0	0	0	0	0	0	0	0	0	0	0	—	—
0	0	0	0	0	0	0	0	0	0	1	1	—	—
0	0	0	0	0	0	0	0	0	1	0	2	—	—
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	0	0	0	0	0	1	1	1	7	—	—
0	0	0	0	0	0	0	1	0	0	0	8	4/8	4
0	0	0	0	0	0	0	1	0	0	1	9	4/8	4
0	0	0	0	0	0	0	1	0	1	0	10	5/10	5
0	0	0	0	0	0	0	1	0	1	1	11	5/10	5
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	0	1	0	0	1012	506/1012	506
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	0	0	0	2024	1012/2024	1012

CK : CLOCK

CLR* : RESET PULSE FOR INTERNAL DIVIDED CLOCK (CXD8875AR)

D15 - D0 : DIGITAL INPUT SIGNAL

G : LATCH PULSE OF DELAY DIRECT CONTROL

G	LATCH PULSE
0	C11-C0 SAMPLE
1	C11-C0 HOLD

INV* : CLOCK TURN OVER CONTROL (CXD8875R)

INV	CLOCK
0	NOT INVERSION ⌐‾|_
1	INVERSION _|‾¬

M0, M1 : MODE CONTROL

M1	M0	MODE
0	0	LONG : 12-BIT, 0 to 2024CK DELAY LINE
0	1	DOUBLE : 12-BIT, 4 to 1012CK AND ×2 DELAY LINE
1	0	WIDE : 16-BIT, 4 to 1012CK DELAY LINE
1	1	———————————————

M2 : MODE CONTROL

M2	MODE
0	DIRECT CONTROL(C EFFECTIVE)
1	PULSE CONTROL(RST EFFECTIVE)

$\overline{OE}$: TRY STATE CONTROL FOR Q15 - Q0 (0 : ENABLE 1 : DISABLE)

RST : RESET PULSE

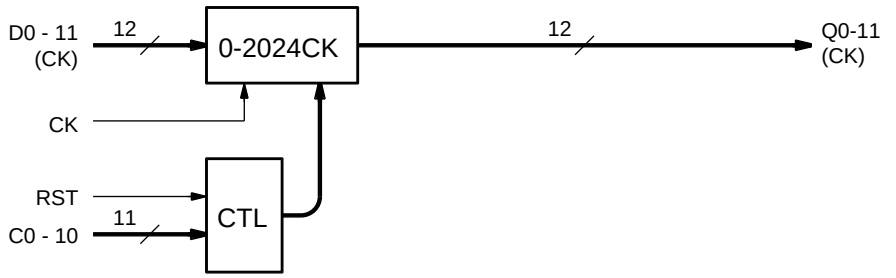
OUTPUT

Q15 - Q0 : DIGITAL OUTPUT SIGNAL

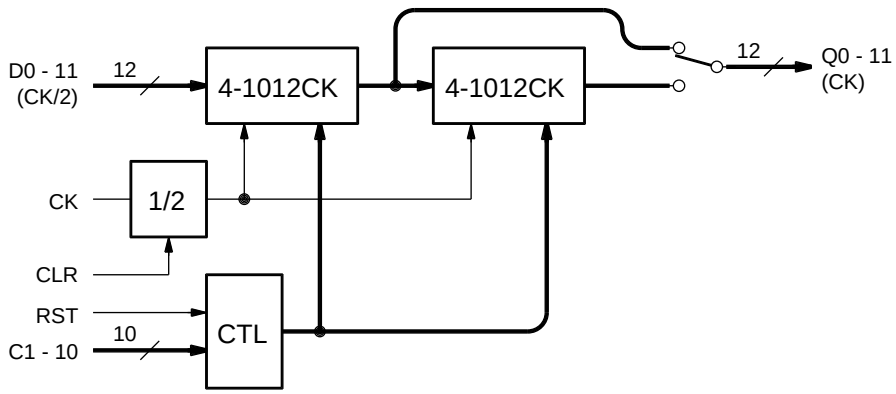
TSTO : TEST TERMINAL

M0, M1

LONG MODE



DOUBLE MODE



WIDE MODE