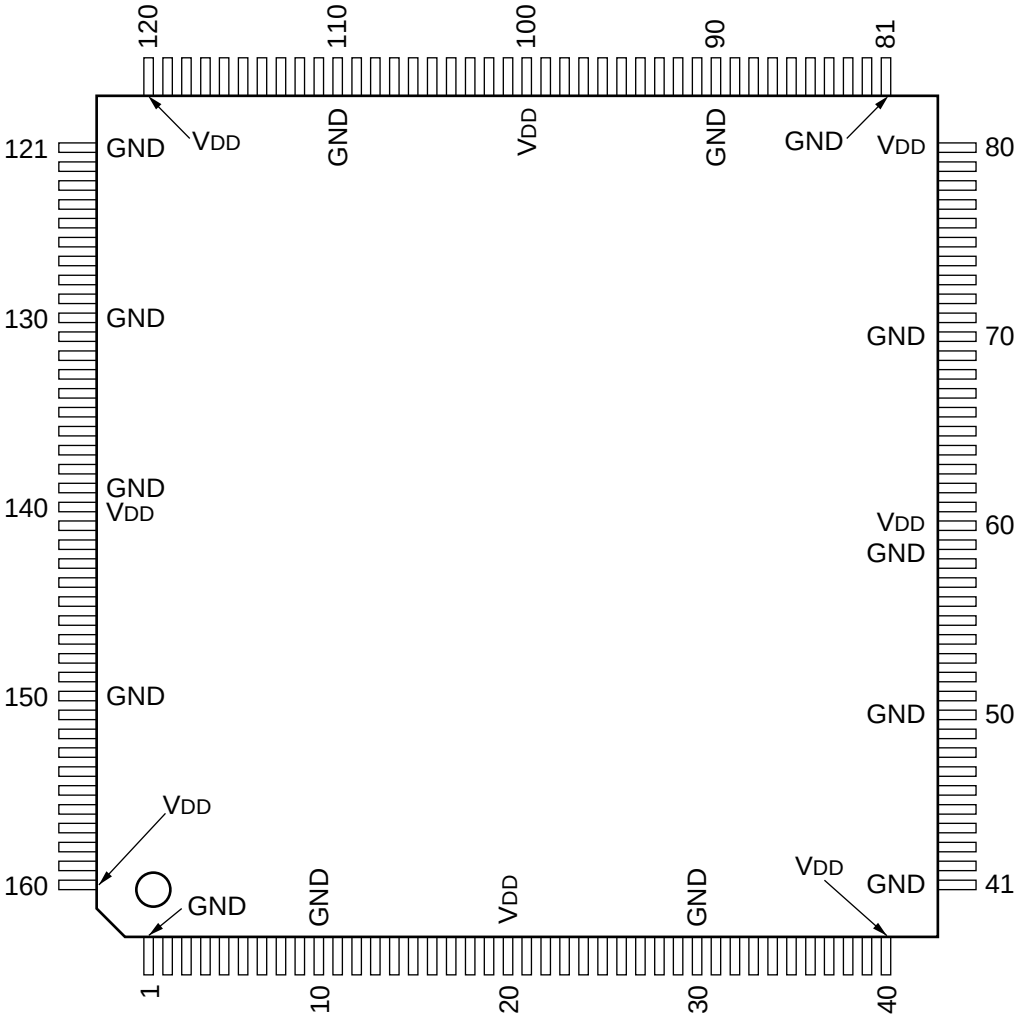
C-MOS KEY PROCESSOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	41	—	GND	81	—	GND	121	—	GND
2	I	$\overline{RST}$	42	O	KEY2 6	82	O	KEY1 3	122	O	VIDEO 2
3	I	TEST 1	43	O	KEY2 5	83	O	KEY1 4	123	O	VIDEO 3
4	I	TEST 0	44	O	KEY2 4	84	O	KEY1 5	124	O	VIDEO 4
5	I	MSRC 14	45	O	KEY2 3	85	O	KEY1 6	125	O	VIDEO 5
6	I	MSRC 13	46	O	KEY2 2	86	O	KEY1 7	126	O	VIDEO 6
7	I	MSRC 12	47	O	KEY2 1	87	O	KEY1 8	127	O	VIDEO 7
8	I	MSRC 11	48	O	KEY2 0	88	O	KEY1 9	128	O	VIDEO 8
9	I	MSRC 10	49	I	DLKY 11	89	O	KEY1 10	129	O	VIDEO 9
10	—	GND	50	—	GND	90	—	GND	130	—	GND
11	I	MSRC 9	51	I	DLKY 10	91	O	KEY1 11	131	O	VIDEO 10
12	I	MSRC 8	52	I	DLKY 9	92	I	BORD 0	132	O	VIDEO 11
13	I	MSRC 7	53	I	DLKY 8	93	I	BORD 1	133	I	KSRC 14
14	I	MSRC 6	54	I	DLKY 7	94	I	BORD 2	134	I	KSRC 13
15	I	MSRC 5	55	I	DLKY 6	95	I	BORD 3	135	I	KSRC 12
16	I	MSRC 4	56	I	DLKY 5	96	I	BORD 4	136	I	KSRC 11
17	I	MSRC 3	57	I	DLKY 4	97	I	BORD 5	137	I	KSRC 10
18	I	MSRC 2	58	I	DLKY 3	98	I	BORD 6	138	I	KSRC 9
19	I	MSRC 1	59	—	GND	99	I	BORD 7	139	—	GND
20	—	V_{DD}	60	—	V_{DD}	100	—	V_{DD}	140	—	V_{DD}
21	I	MSRC 0	61	I	DLKY 2	101	I	BORD 8	141	I	KSRC 8
22	I	MASK 11	62	I	DLKY 1	102	I	BORD 9	142	I	KSRC 7
23	I	MASK 10	63	I	DLKY 0	103	I	BORD 10	143	I	KSRC 6
24	I	MASK 9	64	I	BDKY 11	104	I	BORD 11	144	I	KSRC 5
25	I	MASK 8	65	I	BDKY 10	105	I	FILL 0	145	I	KSRC 4
26	I	MASK 7	66	I	BDKY 9	106	I	FILL 1	146	I	KSRC 3
27	I	MASK 6	67	I	BDKY 8	107	I	FILL 2	147	I	KSRC 2
28	I	MASK 5	68	I	BDKY 7	108	I	FILL 3	148	I	KSRC 1
29	I	MASK 4	69	I	BDKY 6	109	I	FILL 4	149	I	KSRC 0
30	—	GND	70	—	GND	110	—	GND	150	—	GND
31	I	MASK 3	71	I	BDKY 5	111	I	FILL 5	151	I	CK
32	I	MASK 2	72	I	BDKY 4	112	I	FILL 6	152	I	CTMG
33	I	MASK 1	73	I	BDKY 3	113	I	FILL 7	153	I	BLANK
34	I	MASK 0	74	I	BDKY 2	114	I	FILL 8	154	I	CKX
35	O	KEY2 11	75	I	BDKY 1	115	I	FILL 9	155	I	CS1
36	O	KEY2 10	76	I	BDKY 0	116	I	FILL 10	156	I	CS0
37	O	KEY2 9	77	O	KEY1 0	117	I	FILL 11	157	I/O	SDAT
38	O	KEY2 8	78	O	KEY1 1	118	O	VIDEO 0	158	I	SADD
39	O	KEY2 7	79	O	KEY1 2	119	O	VIDEO 1	159	I	CKD
40	—	V_{DD}	80	—	V_{DD}	120	—	V_{DD}	160	—	V_{DD}

INPUT

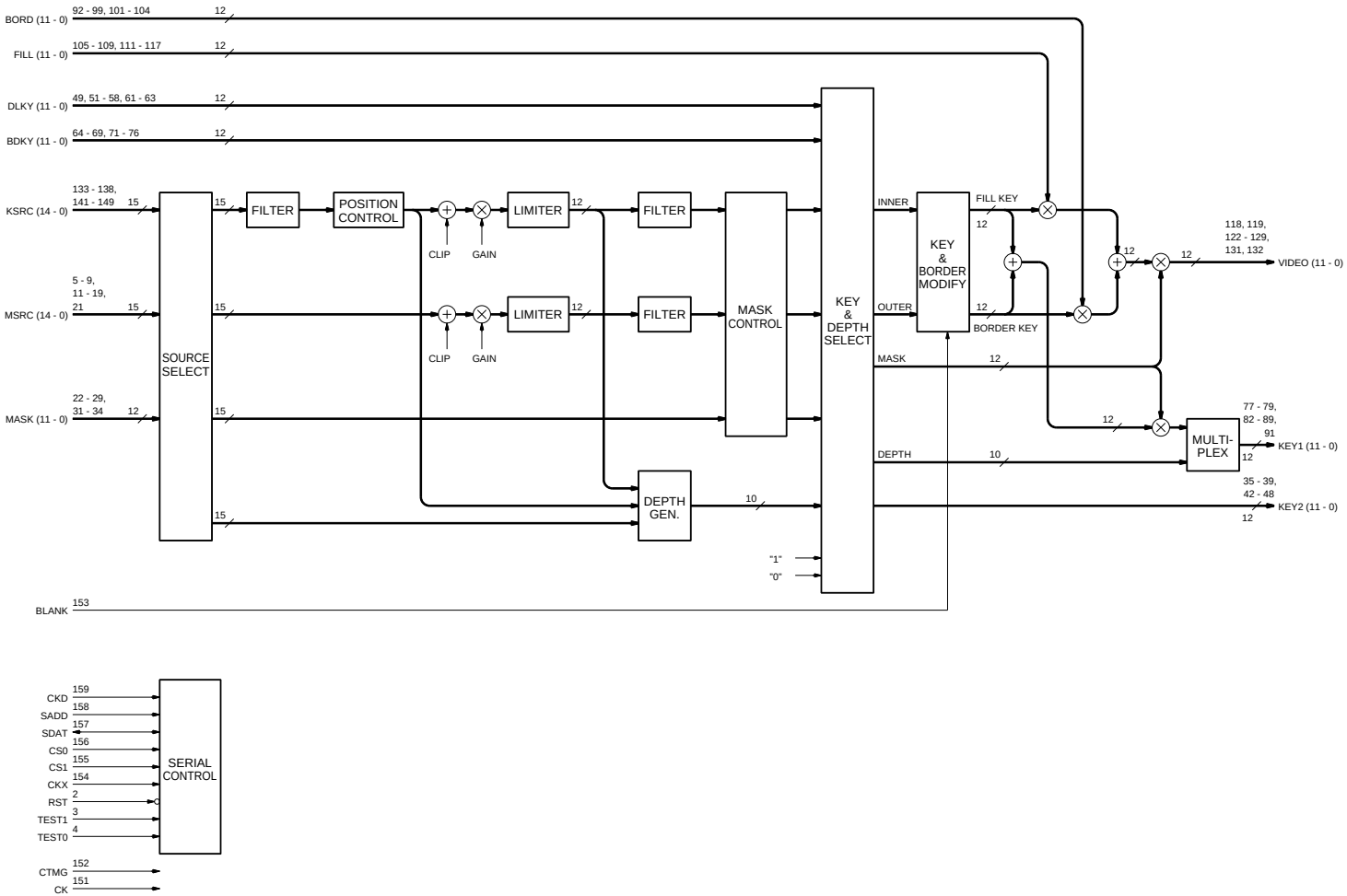
BDKY (11 - 0)	;	BORDER KEY FROM BORDER PROCESSOR (1.11BIT KEY SIGNAL)
BLANK	;	BLANKING PULSE
BORD (11 - 0)	;	BORDER VIDEO (12BIT)
CK	;	SYSTEM CLOCK
CKD	;	SERIAL CONTROL CLOCK
CKX	;	SWITCHING TIMING PULSE
CS1, CS0	;	CHIP SELECT
CTMG	;	COLOR TIMING
DLKY (11 - 0)	;	DELAYED KEY FROM BORDER PROCESSOR (1.11BIT KEY SIGNAL)
FILL (11 - 0)	;	FILL VIDEO (12BIT)
KSRC (14 - 0)	;	KEY SOURCE (2'S COMPLEMENT 15BIT)
MASK (11 - 0)	;	MASK KEY (1.11BIT KEY SIGNAL)
MSRC (14 - 0)	;	MASK SOURCE (2'S COMPLEMENT 15BIT)
$\overline{\text{RST}}$	;	RESET PULSE
SADD	;	SERIAL ADDRESS
TEST 1, TEST 0	;	TEST MODE SET

OUTPUT

KEY1(11 - 0)	;	PROCESSED KEY AND BORDER (1.11BIT KEY SIGNAL)
KEY2(11 - 0)	;	KEY OUT FOR BORDER PROCESSOR (1.11BIT KEY SIGNAL)
VIDEO(11 - 0)	;	PROCESSED VIDEO FILL AND BORDER

INPUT/OUTPUT

SDAT	;	SERIAL DATA


BORD (11 - 0)
92 - 99, 101 - 104
12
FILL (11 - 0)
105 - 109, 111 - 117
12
DLKY (11 - 0)
49, 51 - 58, 61 - 63
12
BDKY (11 - 0)
64 - 69, 71 - 76
12
KSRC (14 - 0)
133 - 138, 141 - 149
15
MSRC (14 - 0)
5 - 9, 11 - 19, 21
15
MASK (11 - 0)
22 - 29, 31 - 34
12
SOURCE SELECT
FILTER
POSITION CONTROL
CLIP
GAIN
LIMITER
FILTER
DEPTH GEN.
10
MASK CONTROL
"1"
"0"
KEY & DEPTH SELECT
INNER
OUTER
MASK
DEPTH
KEY & BORDER MODIFY
FILL KEY
BORDER KEY
MULTI-PLEX
118, 119, 122 - 129, 131, 132
VIDEO (11 - 0)
77 - 79, 82 - 89, 91
KEY1 (11 - 0)
35 - 39, 42 - 48
KEY2 (11 - 0)
BLANK
153

CKD
159
SADD
158
SDAT
157
CS0
156
CS1
155
CKX
154
RST
2
TEST1
3
TEST0
4
CTMG
152
CK
151
SERIAL CONTROL