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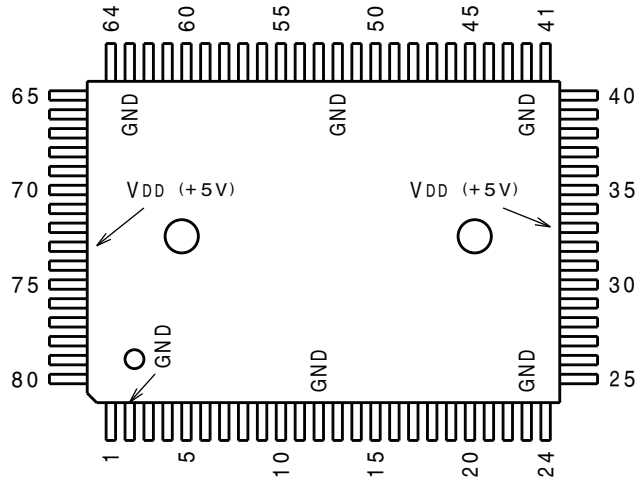
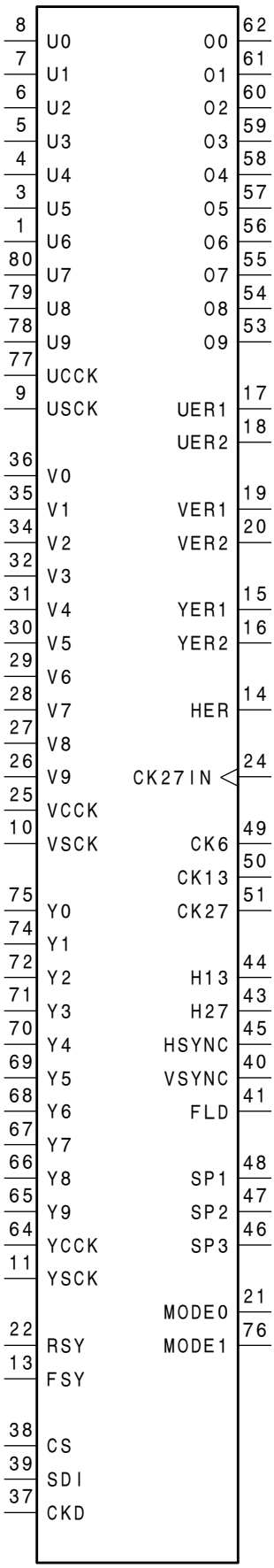
C-MOS AD PROCESSOR

-TOP VIEW-



(VDD=+5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	U6	21	I	MODE1	41	O	FLD	61	O	O1
2	-	GND	22	I	RSY	42	-	GND	62	O	O0
3	I	U5	23	-	GND	43	O	H27	63	-	GND
4	I	U4	24	I	CK27IN	44	I	H13	64	O	YCCK
5	I	U3	25	O	VCCK	45	O	HSYNC	65	I	Y9
6	I	U2	26	I	V9	46	O	SP3	66	I	Y8
7	I	U1	27	I	V8	47	O	SP2	67	I	Y7
8	I	U0	28	I	V7	48	O	SP1	68	I	Y6
9	O	USCK	29	I	V6	49	O	CK6	69	I	Y5
10	O	VSCK	30	I	V5	50	O	CK13	70	I	Y4
11	O	YSCK	31	I	V4	51	O	CK27	71	I	Y3
12	-	GND	32	I	V3	52	-	GND	72	I	Y2
13	I	FSY	33	-	VDD	53	O	O9	73	-	VDD
14	O	HER	34	I	V2	54	O	O8	74	I	Y1
15	O	YER1	35	I	V1	55	O	O7	75	I	Y0
16	O	YER2	36	I	V0	56	O	O6	76	I	MODE0
17	O	UER1	37	I	CKD	57	O	O5	77	O	UCCK
18	O	UER2	38	I	CS	58	O	O4	78	I	U9
19	O	VER1	39	I	SDI	59	O	O3	79	I	U8
20	O	VER2	40	O	VSYNC	60	O	O2	80	I	U7

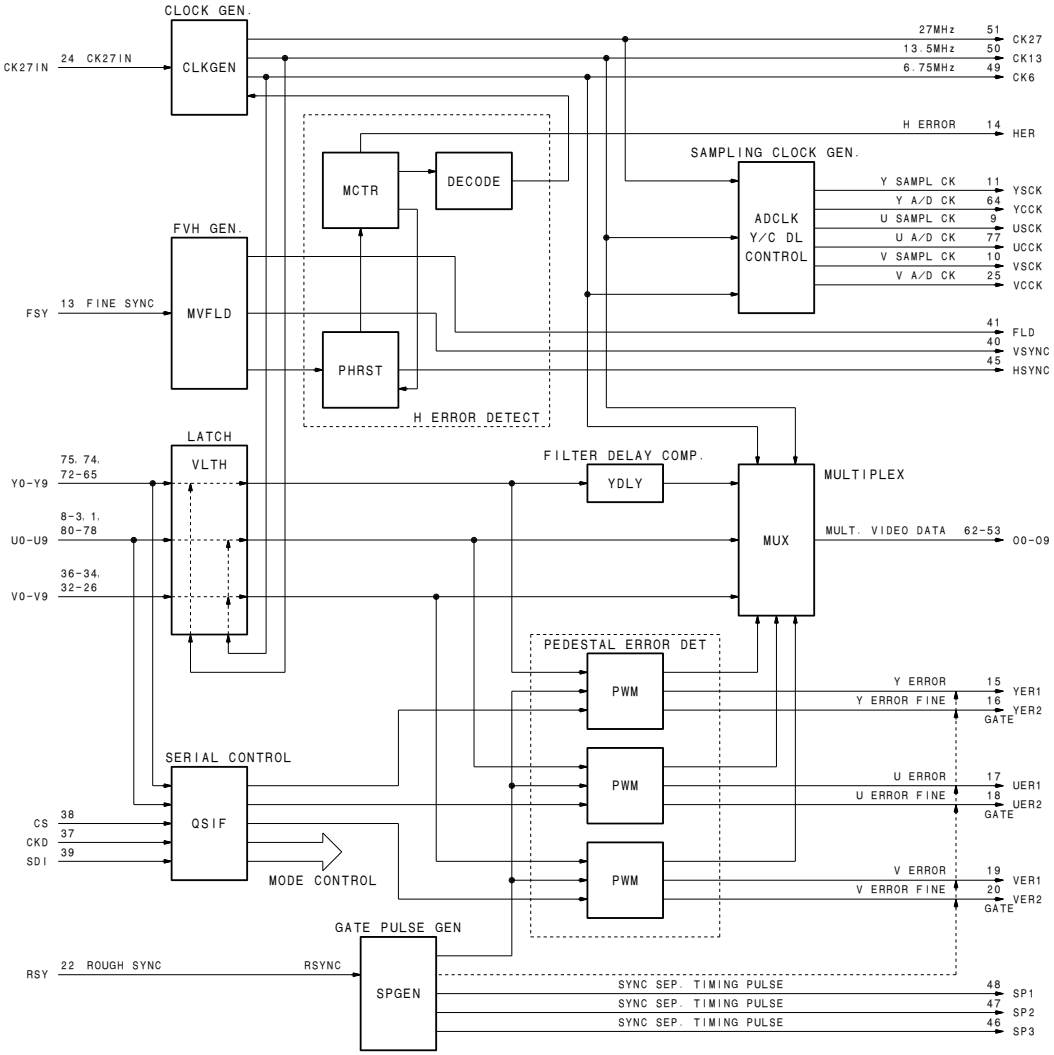


INPUT

CK27IN	;27MHz CLOCK (PLL VCO RETURN)
CKD	;CLOCK FOR SERIAL CONTROL
CS	;CHIP SELECT FOR SERIAL CONTROL
FSY	;SEPALATED SYNC
H13	;H RESET (ENABLE)
MODE0, 1	;TEST MODE CONTROL
RSY	;ROUGH SEPALATED SYNC
SDI	;SERIAL CONTROL DATA
U0-U9	;U DATA (A/D CONV. OUT)
V0-V9	;V DATA (A/D CONV. OUT)
Y0-Y9	;Y DATA (A/D CONV. OUT)

OUTPUT

CK6	;6.75MHz CLOCK
CK13	;13.5MHz CLOCK
CK27	;27MHz CLOCK
FLD	;FIELD ID
H27	;H RESET (LATCHED BY 27MHz)
HER	;H PLL ERROR
HSYNC	;H DRIVE
O0-O9	;MULTIPLEX
SP1, 2, 3	;SYNC SEP. PULSE
UER1, 2	;U PEDESTAL ERROR
VER1, 2	;V PEDESTAL ERROR
VSYNC	;V DRIVE
YC, UC, VCCK	;CONV. CLOCK (FOR A/D CONV.)
YER1, 2	;Y PEDESTAL ERROR
YS, US, VSCK	;SAMPLING CLOCK


CLOCK GEN.
CK27IN
24 CK27IN
CLKGEN
27MHz
51
CK27
13.5MHz
50
CK13
6.75MHz
49
CK6
H ERROR
14
HER
SAMPLING CLOCK GEN.
MCTR
DECODE
ADCLK
Y/C DL
CONTROL
Y SAMPL CK
11
YSCK
Y A/D CK
64
YCCK
U SAMPL CK
9
USCK
U A/D CK
77
UCCK
V SAMPL CK
10
VSCK
V A/D CK
25
VCCK
FVH GEN.
FSY
13 FINE SYNC
MVFLD
PHRST
41
FLD
40
VSYNC
45
HSYNC
H ERROR DETECT
LATCH
VLTH
75. 74.
72-65
Y0-Y9
8-3. 1.
80-78
U0-U9
36-34.
32-26
V0-V9
FILTER DELAY COMP.
YDLY
MULTIPLEX
MUX
MULT. VIDEO DATA
62-53
O0-O9
PEDESTAL ERROR DET
PWM
PWM
PWM
Y ERROR
15
YER1
Y ERROR FINE
16
YER2
GATE
U ERROR
17
UER1
U ERROR FINE
18
UER2
GATE
V ERROR
19
VER1
V ERROR FINE
20
VER2
GATE
SERIAL CONTROL
QSIF
CS
38
CKD
37
SDI
39
MODE CONTROL
GATE PULSE GEN
RSY
22 ROUGH SYNC
RSYNC
SPGEN
SYNC SEP. TIMING PULSE
48
SP1
SYNC SEP. TIMING PULSE
47
SP2
SYNC SEP. TIMING PULSE
46
SP3