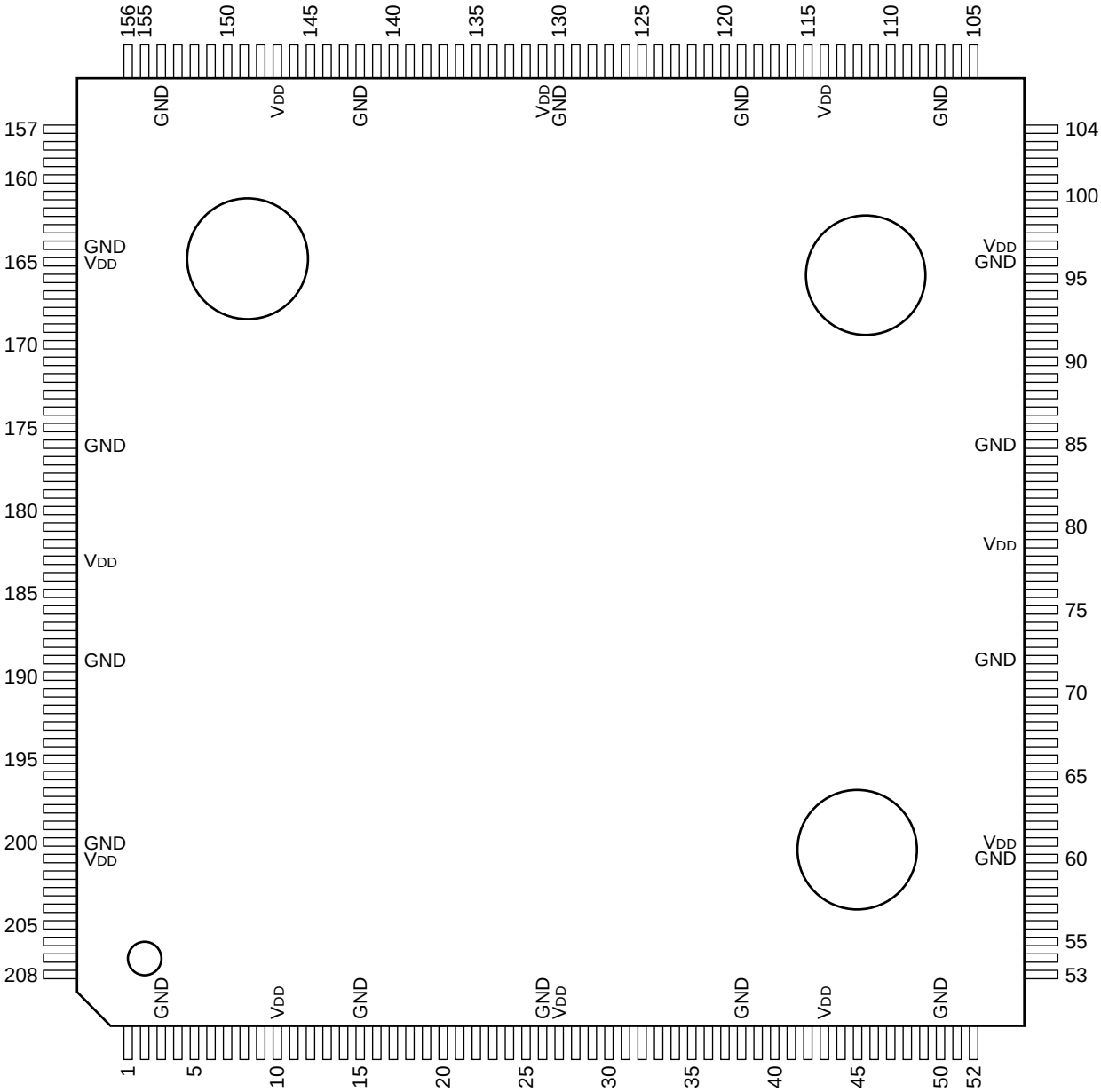
C-MOS WIPE/BOX/MATTE/WASH

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	WASH13	43	—	V_{DD}	85	—	GND	127	I	MOD24	169	I	SADD
2	O	WASH12	44	I	SC1	86	I/O	K/X23	128	I	MOD25	170	I	XMM
3	—	GND	45	I	VBLK1	87	I/O	K/X24	129	I	MOD26	171	I	CKD
4	O	WASH11	46	I	$\overline{CS10}$	88	I/O	K/X25	130	—	GND	172	I	CKX
5	O	WASH10	47	I	$\overline{CS11}$	89	I/O	K/X26	131	—	V_{DD}	173	I	MODW1
6	O	BXWP111	48	I/O	K/X1M2	90	I/O	K/X27	132	I	MOD27	174	I	MODW2
7	O	BXWP110	49	I/O	K/X1M1	91	I/O	K/X28	133	I	MOD28	175	I	CK
8	O	BXWP19	50	—	GND	92	I/O	K/X29	134	I	MOD29	176	—	GND
9	O	BXWP18	51	I/O	K/X10	93	I/O	K/X210	135	I	MOD210	177	I	$\overline{RST}$
10	—	V_{DD}	52	I/O	K/X11	94	I/O	K/X211	136	I	MOD211	178	I	TSI0
11	O	BXWP17	53	I/O	K/X12	95	I/O	V/Y2M1	137	O	BXWP211	179	I	TSI1
12	O	BXWP16	54	I/O	K/X13	96	—	GND	138	O	BXWP210	180	I	TSI2
13	O	BXWP15	55	I/O	K/X14	97	—	V_{DD}	139	O	BXWP29	181	I	TSI3
14	O	BXWP14	56	I/O	K/X15	98	I/O	V/Y20	140	O	BXWP28	182	I	TSM0
15	—	GND	57	I/O	K/X16	99	I/O	V/Y21	141	O	BXWP27	183	—	V_{DD}
16	O	BXWP13	58	I/O	K/X17	100	I/O	V/Y22	142	—	GND	184	I	TSM1
17	O	BXWP12	59	I/O	K/X18	101	I/O	V/Y23	143	O	BXWP26	185	I	TSM2
18	O	BXWP11	60	—	GND	102	I/O	V/Y24	144	O	BXWP25	186	I	TSM3
19	O	BXWP10	61	—	V_{DD}	103	I/O	V/Y25	145	O	BXWP24	187	I	TSM4
20	O	BXWP1M1	62	I/O	K/X19	104	I/O	V/Y26	146	O	BXWP23	188	I	TSCK
21	O	BXWP1M2	63	I/O	K/X110	105	I/O	V/Y27	147	—	V_{DD}	189	—	GND
22	I	MOD10	64	I/O	K/X111	106	I/O	V/Y28	148	O	BXWP22	190	I	D1/D2
23	I	MOD11	65	I/O	V/Y1M1	107	—	GND	149	O	BXWP21	191	I	CS/CP
24	I	MOD12	66	I/O	V/Y10	108	I/O	V/Y29	150	O	BXWP20	192	I	TMODE
25	I	MOD13	67	I/O	V/Y11	109	I/O	V/Y210	151	O	BXWP2M1	193	O	TSO5
26	—	GND	68	I/O	V/Y12	110	I/O	V/Y211	152	O	BXWP2M2	194	O	TSO4
27	—	V_{DD}	69	I/O	V/Y13	111	I	MPXCTL2	153	O	WASH211	195	O	TSO3
28	I	MOD14	70	I/O	V/Y14	112	I	$\overline{OEBL2}$	154	—	GND	196	O	TSO2
29	I	MOD15	71	I/O	V/Y15	113	I	$\overline{OEWL2}$	155	O	WASH210	197	O	TSO1
30	I	MOD16	72	—	GND	114	—	V_{DD}	156	O	WASH29	198	O	TSO0
31	I	MOD17	73	I/O	V/Y16	115	I	HD2	157	O	WASH28	199	O	WASH111
32	I	MOD18	74	I/O	V/Y17	116	I	VD2	158	O	WASH27	200	—	GND
33	I	MOD19	75	I/O	V/Y18	117	I	FLOE2	159	O	WASH26	201	-	V_{DD}
34	I	MOD110	76	I/O	V/Y19	118	I	SC2	160	O	WASH25	202	O	WASH110
35	I	MOD111	77	I/O	V/Y110	119	—	GND	161	O	WASH24	203	O	WASH19
36	I	MPXCTL1	78	I/O	V/Y111	120	I	VBLK2	162	O	WASH23	204	O	WASH18
37	I	$\overline{OEBL1}$	79	—	V_{DD}	121	I	$\overline{CS20}$	163	O	WASH22	205	O	WASH17
38	—	GND	80	I/O	K/X2M2	122	I	$\overline{CS21}$	164	—	GND	206	O	WASH16
39	I	$\overline{OEWL1}$	81	I/O	K/X2M1	123	I	MOD20	165	—	V_{DD}	207	O	WASH15
40	I	HD1	82	I/O	K/X20	124	I	MOD21	166	O	WASH21	208	O	WASH14
41	I	VD1	83	I/O	K/X21	125	I	MOD22	167	O	WASH20			
42	I	FLOE1	84	I/O	K/X22	126	I	MOD23	168	I/O	SDAT			

INPUT

(WASH-CHANNEL-1)

$\overline{CS1}$ ($\overline{1}$, $\overline{0}$) ; CHIP SELECT
FLOE1 ; FIELD ODD/EVEN INPUT
HD1 ; H DRIVE INPUT
MOD1 (11 - 0) ; MODULATION INPUT
MODW1 ; WIPE/MATTE MODE INPUT (L = MATTE, H = WIPE)
MPX CTL 1 ; MODULATION H/V SWITCH PULSE INPUT
$\overline{OEBL1}$; OUTPUT ENABLE INPUT FOR BXWP1
$\overline{OEWL1}$; OUTPUT ENABLE INPUT FOR WASH1
SC1 ; SUB CARRIER INPUT
VBLK1 ; BLANKING PULSE INPUT
VD1 ; V DRIVE INPUT

(WASH-CHANNEL-2)

$\overline{CS2}$ ($\overline{1}$, $\overline{0}$) ; CHIP SELECT
FLOE2 ; FIELD ODD/EVEN INPUT
HD2 ; H DRIVE INPUT
MOD2 (11-0) ; MODULATION INPUT
MODW2 ; WIPE/MATTE MODE INPUT (L = MATTE, H = WIPE)
MPX CTL 2 ; MODULATION H/V SWITCH PULSE INPUT
$\overline{OEBL2}$; OUTPUT ENABLE INPUT FOR BXWP1
$\overline{OEWL2}$; OUTPUT ENABLE INPUT FOR WASH1
SC2 ; SUB CARRIER INPUT
VBLK2 ; BLANKING PULSE INPUT
VD2 ; V DRIVE INPUT

(COMMON)

CK ; 27 MHz CLOCK INPUT
CKD ; CLOCK INPUT FOR SERIAL CONTROL
CKX ; SWITCHING TIMING PULSE INPUT
CS/CP ; COMPOSITE/COMPONENT MODE (L = COMPOSITE, H = COMPONENT)
D1/D2 ; D1/D2 MODE (L = D1, H = D2)
$\overline{RST}$; RESET INPUT FOR CHIP (L = RESET)
SADD ; ADDRESS INPUT FOR SERIAL CONTROL
SDAT ; DATA INPUT FOR SERIAL CONTROL

(TEST PIN FOR IC CHECK)

TMODE ; TEST MODE (H = TEST MODE)
TSCK ; CLOCK FOR TEST
TSI (3 - 0) ; INPUT FOR TEST
TSM (4 - 0) ; INPUT FOR MULTIPLIER CHECK
XMM ; MULTIPLIER CHECK MODE (H = CHECK)

OUTPUT

(WASH-CHANNEL-1)

BXWP1 (11 - 0) ; BOX/WIPE KEY OUTPUT
WASH1 (11 - 0) ; WASH VIDEO OUTPUT

(WASH-CHANNEL-1)

BXWP2 (11 - 0) ; BOX/WIPE KEY OUTPUT
WASH2 (11 - 0) ; WASH VIDEO OUTPUT

(COMMON)

TSO (5 - 0) ; OUTPUT FOR TEST

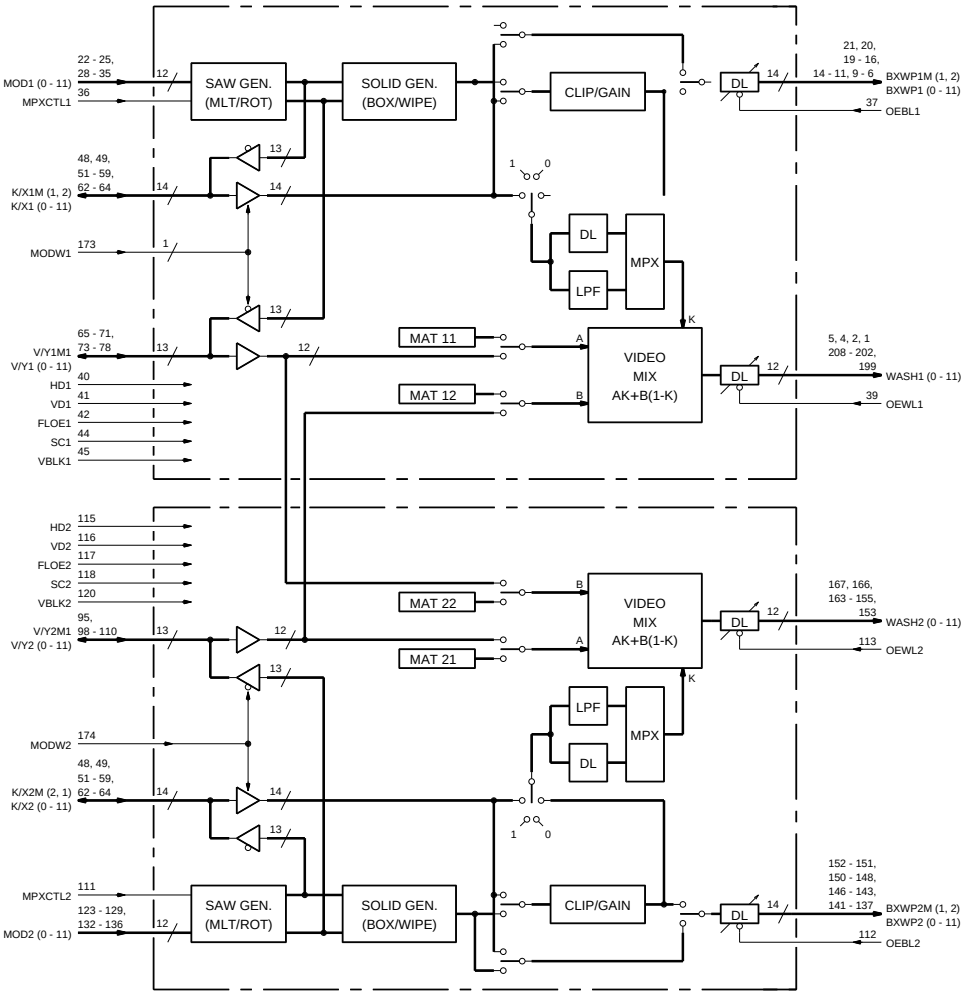
INPUT/OUTPUT

(WASH-CHANNEL-1)

K/X1 (11-M2) ; KEY INPUT/X ADDRESS OUTPUT
(MODW1 : L = KEY INPUT)
V/Y1 (11-M1) ; VIDEO INPUT/Y ADDRESS OUTPUT
(MODW1 : L = VIDEO INPUT)

(WASH-CHANNEL-2)

K/X2 (11-M2) ; KEY INPUT/X ADDRESS OUTPUT
(MODW2 : L = KEY INPUT)
V/Y2 (11-M1) ; VIDEO INPUT/Y ADDRESS OUTPUT
(MODW2 : L = VIDEO INPUT)


MOD1 (0 - 11)
MPXCTL1
22 - 25,
28 - 35
36
12
SAW GEN.
(MLT/ROT)
SOLID GEN.
(BOX/WIPE)
CLIP/GAIN
DL
14
21, 20,
19 - 16,
14 - 11, 9 - 6
BXWP1M (1, 2)
BXWP1 (0 - 11)
37
OEBL1
48, 49,
51 - 59,
62 - 64
K/X1M (1, 2)
K/X1 (0 - 11)
13
14
1
0
MODW1
173
1
DL
LPF
MPX
K
65 - 71,
73 - 78
V/Y1M1
V/Y1 (0 - 11)
MAT 11
MAT 12
A
B
VIDEO
MIX
AK+B(1-K)
12
5, 4, 2, 1
208 - 202,
199
WASH1 (0 - 11)
39
OEWL1
HD1
VD1
FLOE1
SC1
VBLK1
40
41
42
44
45
HD2
VD2
FLOE2
SC2
VBLK2
115
116
117
118
120
MAT 22
MAT 21
167, 166,
163 - 155,
153
WASH2 (0 - 11)
113
OEWL2
95,
98 - 110
V/Y2M1
V/Y2 (0 - 11)
MODW2
174
48, 49,
51 - 59,
62 - 64
K/X2M (2, 1)
K/X2 (0 - 11)
MPXCTL2
111
123 - 129,
132 - 136
MOD2 (0 - 11)
152 - 151,
150 - 148,
146 - 143,
141 - 137
BXWP2M (1, 2)
BXWP2 (0 - 11)
112
OEBL2