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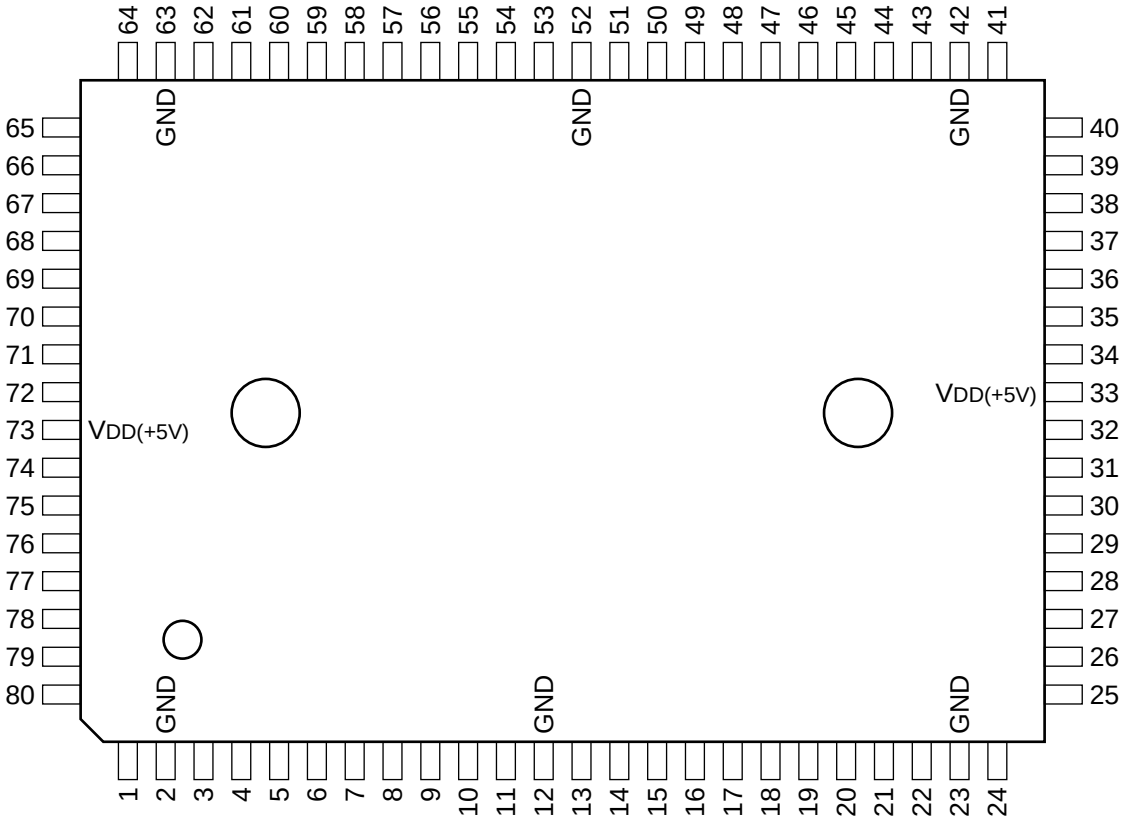
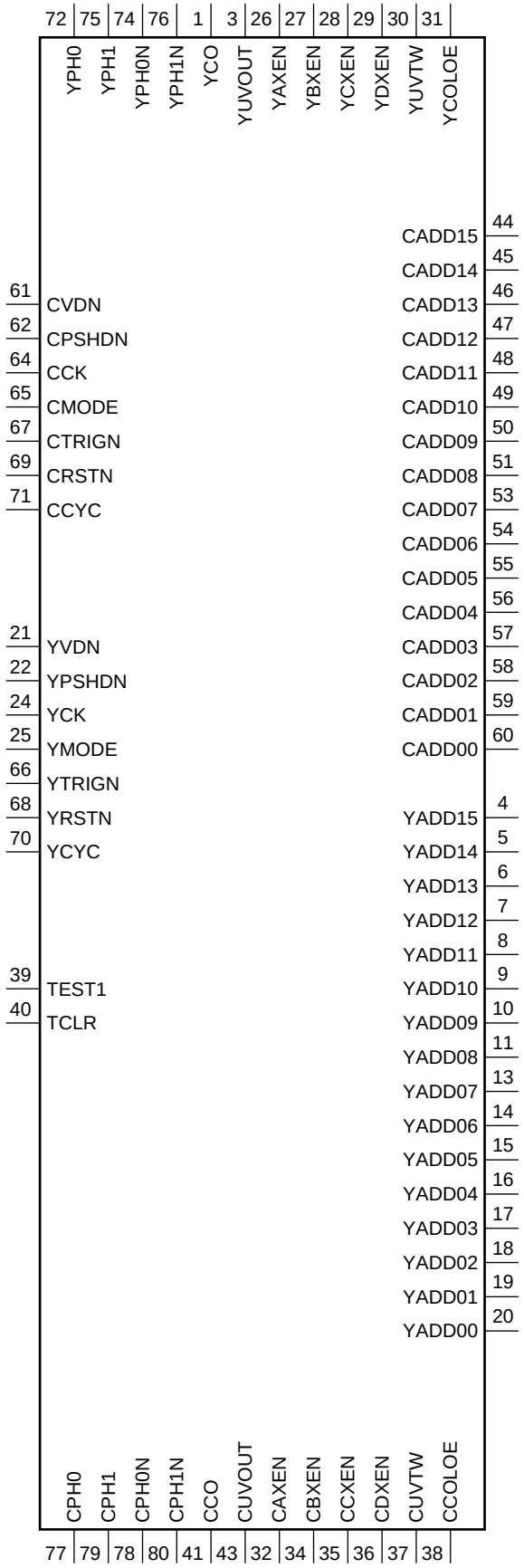
C-MOS SRAM ADDRESS GENERATOR

-TOP VIEW-



(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	YCO	21	I	YVDN	41	O	CCO	61	I	CVDN
2	—	GND	22	I	YPSHDN	42	—	GND	62	I	CPSHDN
3	O	YUVOUT	23	—	GND	43	O	CUVOUT	63	—	GND
4	O	YADD15	24	I	YCK	44	O	CADD15	64	I	CCK
5	O	YADD14	25	I	YMODE	45	O	CADD14	65	I	CMODE
6	O	YADD13	26	O	YAXEN	46	O	CADD13	66	I	YTRIGN
7	O	YADD12	27	O	YBXEN	47	O	CADD12	67	I	CTRIGN
8	O	YADD11	28	O	YCXEN	48	O	CADD11	68	I	YRSTN
9	O	YADD10	29	O	YDXEN	49	O	CADD10	69	I	CRSTN
10	O	YADD09	30	O	YUVTW	50	O	CADD09	70	I	YCYC
11	O	YADD08	31	O	YCOLOE	51	O	CADD08	71	I	CCYC
12	—	GND	32	O	CAXEN	52	—	GND	72	O	YPH0
13	O	YADD07	33	—	V_{DD}	53	O	CADD07	73	—	V_{DD}
14	O	YADD06	34	O	CBXEN	54	O	CADD06	74	O	YPH0N
15	O	YADD05	35	O	CCXEN	55	O	CADD05	75	O	YPH1
16	O	YADD04	36	O	CDXEN	56	O	CADD04	76	O	YPH1N
17	O	YADD03	37	O	CUVTW	57	O	CADD03	77	O	CPH0
18	O	YADD02	38	O	CCOLOE	58	O	CADD02	78	O	CPH0N
19	O	YADD01	39	I	TEST1	59	O	CADD01	79	O	CPH1
20	O	YADD00	40	I	TCLR	60	O	CADD00	80	O	CPH1N

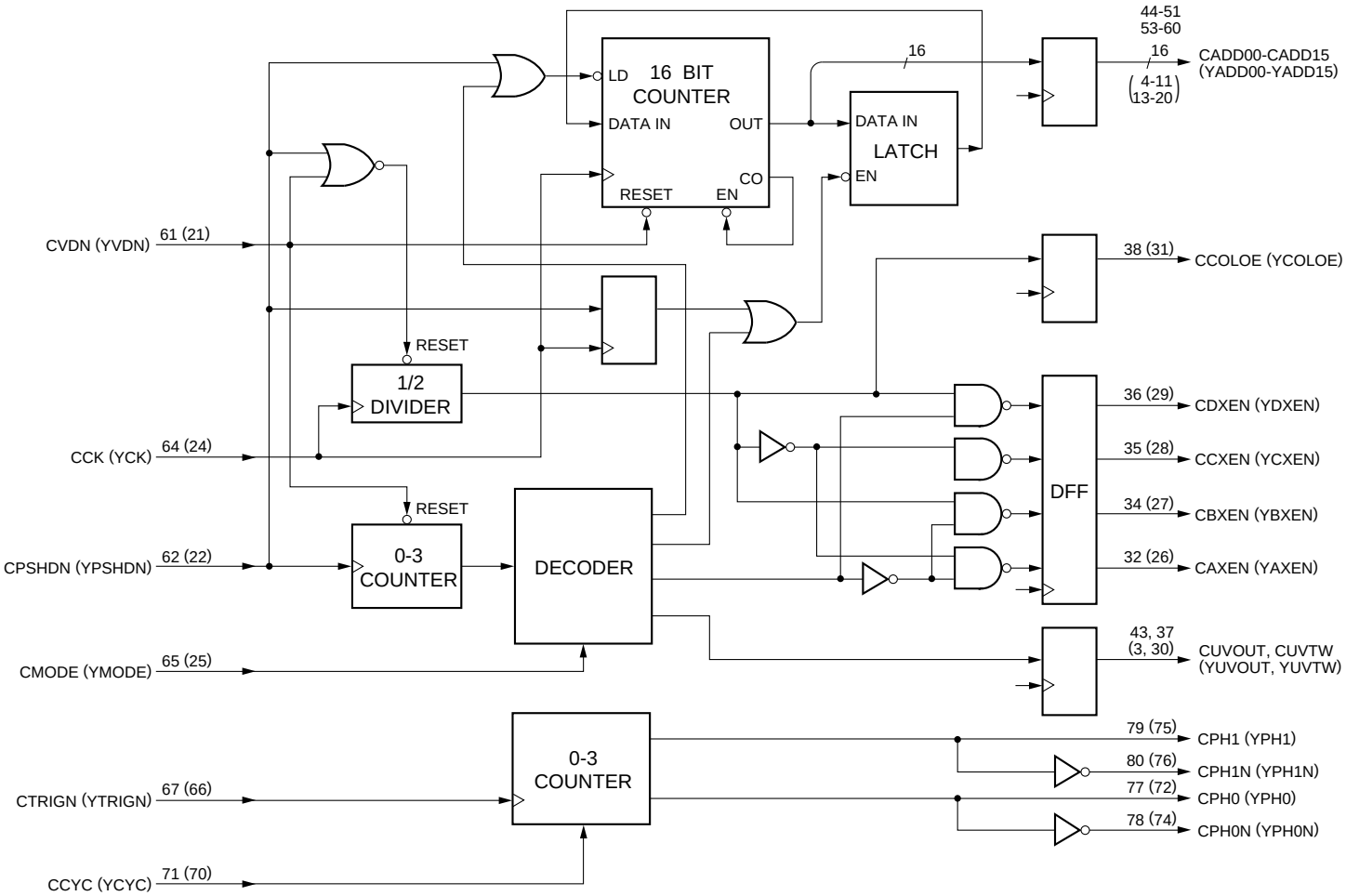


INPUT

CCK	;	CLOCK FOR C
CCYC	;	CYCLIC MODE (C)
CMODE	;	MODE SEL FOR C
CPSHDN	;	PSHDN FOR C
CRSTN	;	CYCLIC RESET (C)
CTRIGN	;	FIELD TRIGGER (C)
CVDN	;	VD FOR C
TCLR	;	TEST
TEST1	;	TEST
YCK	;	CLOCK FOR Y
YCYC	;	CYCLIC MODE (Y)
YMODE	;	MODE SEL FOR Y
YPSHDN	;	PSHDN FOR Y
YRSTN	;	CYCLIC RESET (Y)
YTRIGN	;	FIELD TRIGGER (Y)
YVDN	;	VD FOR Y

OUTPUT

CADD00 - CADD15	;	C ADDRESS
CAXEN	;	C A-BANK ENABLE
CBXEN	;	C B-BANK ENABLE
CCO	;	C COLUMN
CCOLOE	;	C-COLUMN ODD / EVEN
CCXEN	;	C C-BANK ENABLE
CDXEN	;	C D-BANK ENABLE
CPH0	;	3/4 FIELD COUNTER (C)
CPH0N	;	3/4 FIELD COUNTER (C)
CPH1	;	3/4 FIELD COUNTER (C)
CPH1N	;	3/4 FIELD COUNTER (C)
CUVOUT	;	CPSHDN COUNTER
CUVTW	;	CPSHDN COUNTER
YADD00 - YADD15	;	Y ADDRESS
YAXEN	;	Y A-BANK ENABLE
YBXEN	;	Y B-BANK ENABLE
YCO	;	Y COLUMN
YCOLOE	;	Y COLUMN ODD / EVEN
YCXEN	;	Y C-BANK ENABLE
YDXEN	;	Y D-BANK ENABLE
YPH0	;	3/4 FIELD COUNTER (Y)
YPH0N	;	3/4 FIELD COUNTER (Y)
YPH1	;	3/4 FIELD COUNTER (Y)
YPH1N	;	3/4 FIELD COUNTER (Y)
YUVOUT	;	YPSHDN COUNTER
YUVTW	;	YPSHDN COUNTER


LD
16 BIT
COUNTER
DATA IN
OUT
RESET
EN
CO
16
DATA IN
LATCH
EN
44-51
53-60
16
4-11
13-20
CADD00-CADD15
(YADD00-YADD15)
CVDN (YVDN)
61 (21)
38 (31)
CCOLOE (YCOLOE)
RESET
1/2
DIVIDER
CCK (YCK)
64 (24)
36 (29)
CDXEN (YDXEN)
35 (28)
CCXEN (YCXEN)
34 (27)
CBXEN (YBXEN)
32 (26)
CAXEN (YAXEN)
DFF
RESET
CPSHDN (YPSHDN)
62 (22)
0-3
COUNTER
DECODER
CMODE (YMODE)
65 (25)
43, 37
(3, 30)
CUVOUT, CUVTW
(YUVOUT, YUVTW)
0-3
COUNTER
79 (75)
CPH1 (YPH1)
80 (76)
CPH1N (YPH1N)
CTRIGN (YTRIGN)
67 (66)
77 (72)
CPH0 (YPH0)
78 (74)
CPH0N (YPH0N)
CCYC (YCYC)
71 (70)