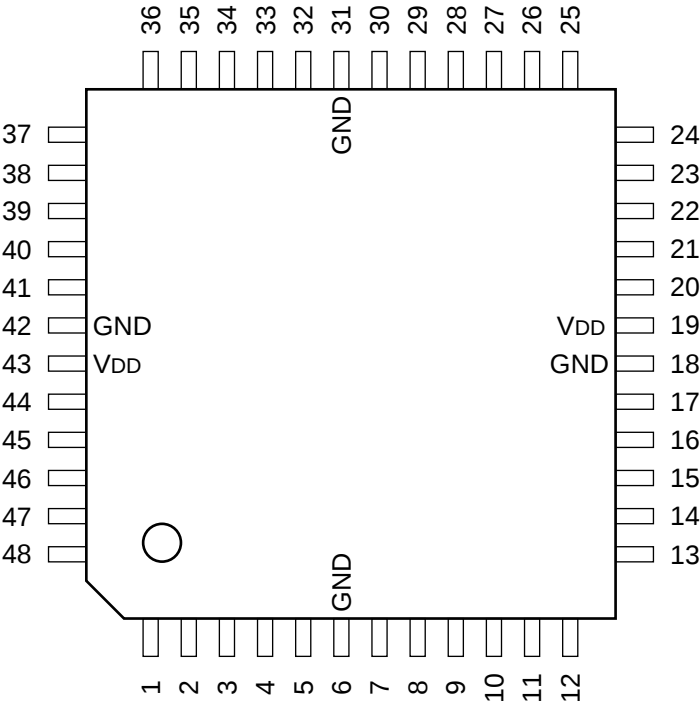


C-MOS D1 SUPERIMPOSER
—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	SLNP	25	O	SIVD 2
2	I	VD 9	26	O	SIVD 3
3	I	VD 8	27	O	SIVD 4
4	I	VD 7	28	O	SIVD 5
5	I	VD 6	29	I	Y WHITE 6
6	—	GND	30	I	Y WHITE 7
7	I	VD 5	31	—	GND
8	I	VD 4	32	I	Y WHITE 8
9	I	VD 3	33	O	SIVD 6
10	I	VD 2	34	O	SIVD 7
11	I	VD 1	35	O	SIVD 8
12	I	VD 0	36	O	SIVD 9
13	I	Y BLK 4	37	O	SEL A
14	I	Y BLK 5	38	O	SEL B
15	I	Y BLK 6	39	O	C FRAME
16	I	Y BLK 7	40	O	Y FRAME
17	I	CK 27	41	O	Y CHARA
18	—	GND	42	—	GND
19	—	VDD	43	—	VDD
20	I	OC 13	44	I	CFR DLY
21	I	OC 6	45	I	Y DLY A
22	O	GP422	46	I	Y DLY B
23	O	SIVD 0	47	I	FRAME
24	O	SIVD 1	48	I	CHARA

2	VD 9	SIVD 9	36
3	VD 8	SIVD 8	35
4	VD 7	SIVD 7	34
5	VD 6	SIVD 6	33
7	VD 5	SIVD 5	28
8	VD 4	SIVD 4	27
9	VD 3	SIVD 3	26
10	VD 2	SIVD 2	25
11	VD 1	SIVD 1	24
12	VD 0	SIVD 0	23
1	SLNP	GP422	22
17	CK 27	SEL A	37
20	OC 13	SEL B	38
21	OC 6		
		C FRAME	39
47	FRAME	Y FRAME	40
48	CHARA	Y CHARA	41
32	Y WHITE 8		
30	Y WHITE 7		
29	Y WHITE 6		
16	Y BLK 7		
15	Y BLK 6		
14	Y BLK 5		
13	Y BLK 4		
44	CFR DLY		
45	Y DLY A		
46	Y DLY B		

INPUT

CFR DLY ; DELAY CONTROL OF C FRAME SIGNAL
 CHARA ; SUPERIMPOSE CHARACTER SIGNAL
 CK 27 ; 27 MHz CLOCK
 FRAME ; SUPER IMPOSE CHARACTER FRAME
 SLNP ; 525/625 LINE SELECTE
 VD 0 - 9 ; DIGITAL VIDEO PARALLEL DATA
 Y BLK 4 - 7 ; Y BLANKING LEVEL
 Y DLY A, B ; DELAY CONTROL OF Y CHARA AND Y FRAME SIGNALS
 Y WHITE 6 - 8 ; Y WHITE LEVEL

OUTPUT

C FRAME ; CHROMA FRAME PULSE
 GP422 ; 4 : 2 : 2 GROUP PULSE
 OC 13 ; 13.5 MHz CLOCK
 OC 6 ; 6.75 MHz CLOCK
 SEL A, B ; SELECTION SIGNAL OF INNER MULTIPLEXER
 SIVD 0 - 9 ; DIGITAL VIDEO PARALLEL DATA AFTER SUPERIMPOSED
 Y CHARA ; Y CHARACTER PULSE
 Y FRAME ; Y FRAME PULSE

SEL		MPX
A	B	
0	0	THROUGH
1	0	Y BLK
0	1	C BLK
1	1	Y WHITE

