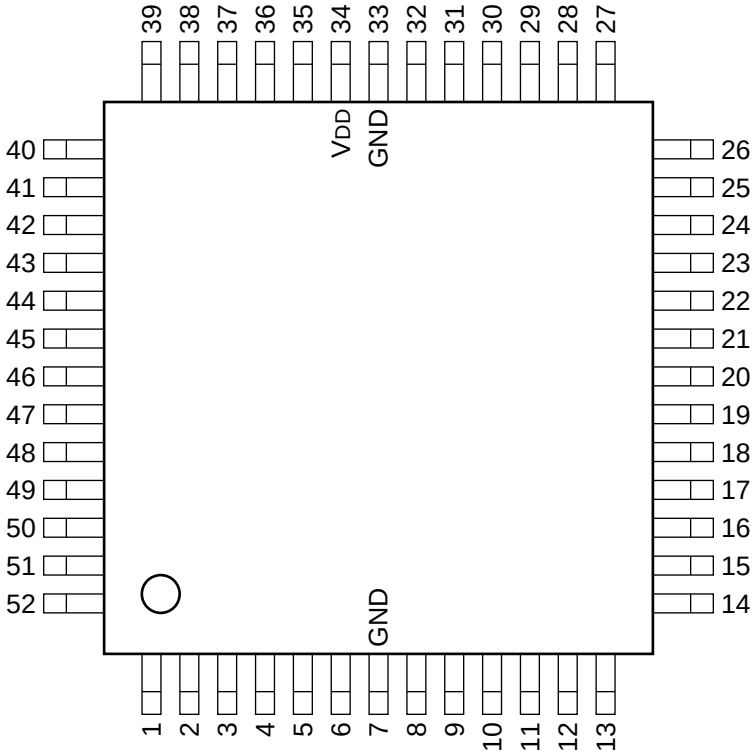
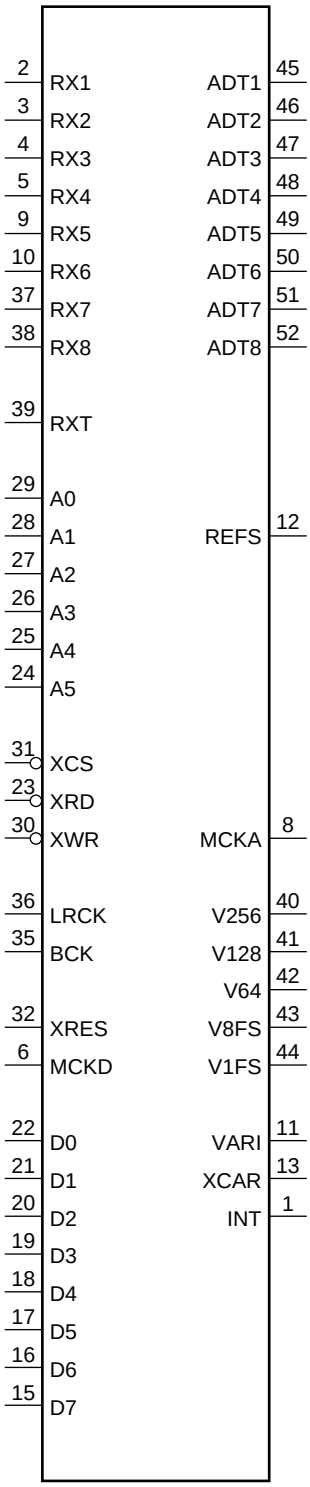
C-MOS DIGITAL MIXER (APX-EL/APX-288/APX-R3)

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	INT	14	—	N.C.	27	I	A2	40	O	V256
2	I	RX1	15	I/O	D7	28	I	A1	41	O	V128
3	I	RX2	16	I/O	D6	29	I	A0	42	O	V64
4	I	RX3	17	I/O	D5	30	I	XWR	43	O	V8FS
5	I	RX4	18	I/O	D4	31	I	XCS	44	O	V1FS
6	I	MCKD	19	I/O	D3	32	I	XRES	45	O	ADT1
7	—	GND	20	I/O	D2	33	—	GND	46	O	ADT2
8	I/O	MCKA	21	I/O	D1	34	—	VDD	47	O	ADT3
9	I	RX5	22	I/O	D0	35	I	BCK	48	O	ADT4
10	I	RX6	23	I	XRD	36	I	LRCK	49	O	ADT5
11	O	VAR1	24	I	A5	37	I	RX7	50	O	ADT6
12	O	REFS	25	I	A4	38	I	RX8	51	O	ADT7
13	O	XCAR	26	I	A3	39	I	RXT	52	O	ADT8



RX1 - RX8	:	AES/EBU DIGITAL AUDIO INPUT CH.1 - CH.8
RXT	:	AES/EBU DIGITAL AUDIO INPUT FOR DIAG.
A0 - A5	:	ADDRESS INPUTS
XCS	:	CHIP SELECT(LOW ACTIVE)
XRD	:	READ(LOW ACTIVE)
XWR	:	WRITE(LOW ACTIVE)
LRCK	:	LR CLOCK(INTERNAL)
BCK	:	64fs CLOCK(INTERNAL)
XRES	:	NAGATIVE PULSE INPUT FOR THE INITIALIZATION
	:	MASTER CLOCK 24.576 MHz FOR INTERNAL DPLL
MCKD	:	DATA INPUTS
D0 - D7	:	AUDIO DATA CH.1 - CH.8
ADT1 - ADT8	:	APLL REF
REFS	:	APLL VCO CLOCK(fo = 24.576 MHz)
MCKA	:	256fs CLOCK IN APLL CIRCUIT
V256	:	128fs CLOCK IN APLL CIRCUIT
V128	:	64fs CLOCK IN APLL CIRCUIT
V64	:	8fs CLOCK IN APLL CIRCUIT
V8FS	:	1fs CLOCK IN APLL CIRCUIT
V1FS	:	APLL VARI
VARI	:	CARRY OUTPUT OF APLL DEVIDER (LOW ACTIVE)
XCAR	:	INTERRUPT FOR THE CONTROLLER (CPU)
INT		