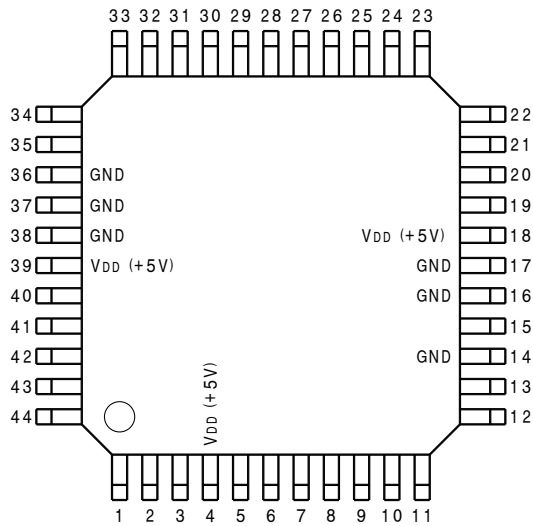
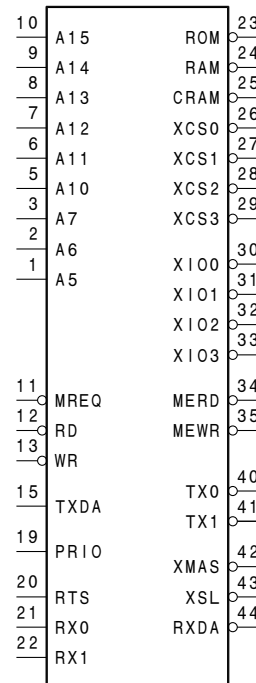

CXD8813Q
IL08

C-MOS GATE ARRAY -TOP VIEW-



(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	A5	23	O	ROM
2	I	A6	24	O	RAM
3	I	A7	25	O	CRAM
4	-	VDD	26	O	XCS0
5	I	A10	27	O	XCS1
6	I	A11	28	O	XCS2
7	I	A12	29	O	XCS3
8	I	A13	30	O	XIO0
9	I	A14	31	O	XIO1
10	I	A15	32	O	XIO2
11	I	MREQ	33	O	XIO3
12	I	XRD	34	O	MERD
13	I	XWR	35	O	MEWR
14	-	GND	36	-	GND
15	I	TXDA	37	-	GND
16	-	GND	38	-	GND
17	-	GND	39	-	VDD
18	-	VDD	40	O	TX0
19	I	PRI0	41	O	TX1
20	I	RTS	42	O	XMAS
21	I	RX0	43	O	XSL
22	I	RX1	44	O	RXDA



INPUT

A5-A15 : ADDRESS INPUT
MREQ : MEMORY REQUEST IN
PRI0 : PRIORITY CONTROL IN
RD : READ IN
RTS : RTS CONTROL IN
RX0 : RX0 IN
RX1 : RX1 IN
TXDA : TX DATA IN
WR : WRITE IN

OUTPUT

CRAM : 4k BYTE ADDRESS DECODE OUTPUT
MERD : MEMORY READ OUTPUT
MEWR : MEMORY WRITE OUTPUT
RAM : 8k BYTE ADDRESS DECODE OUTPUT
ROM : 48k BYTE ADDRESS DECODE OUTPUT
RXDA : SELECTED RX DATA OUTPUT
TX0 : TX DATA OUTPUT -0
TX1 : TX DATA OUTPUT -1
XCS0-XCS3 : 1k BYTE ADDRESS DECODE OUTPUT
XIO0-XIO3 : I/O CHIP SELECT OUTPUT
XMAS : MASTER ENABLE L OUTPUT
XSL : SLAVE ENABLE L OUTPUT