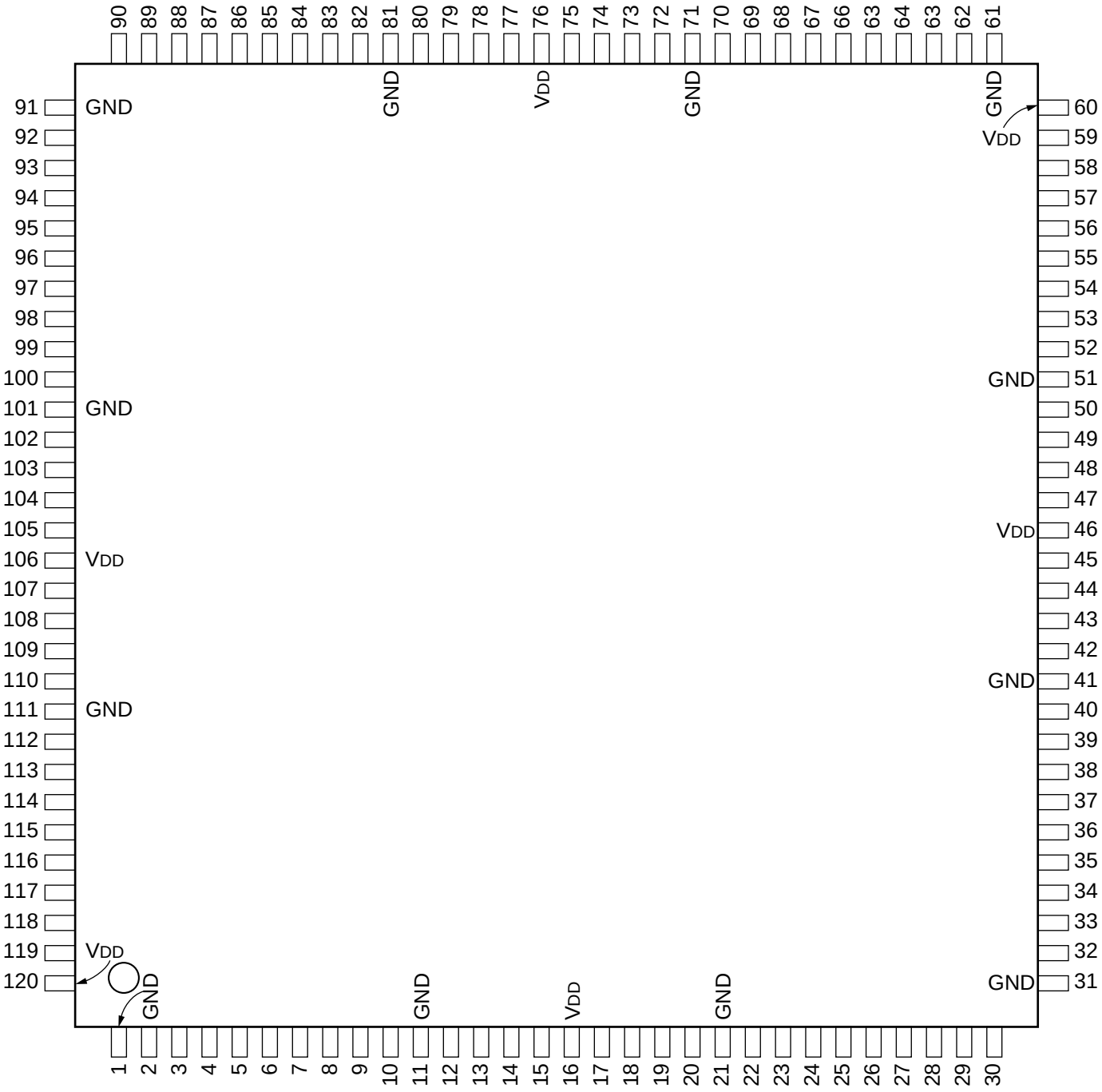
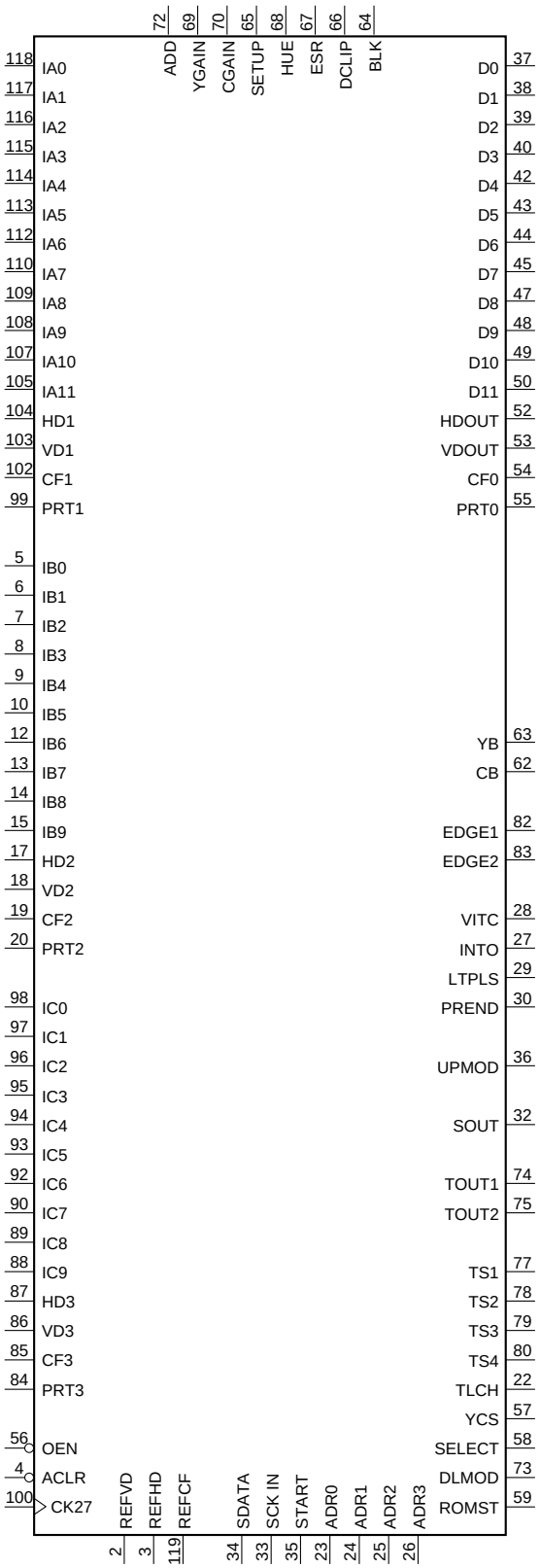
C-MOS VIDEO PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	31	—	GND	61	—	GND	91	—	GND
2	I	REFVD	32	O	SOUT	62	O	CB	92	I	IC6
3	I	REFHD	33	I	SCKIN	63	O	YB	93	I	IC5
4	I	$\overline{\text{ACLR}}$	34	I	SDATA	64	I	BLK	94	I	IC4
5	I	IB0	35	I	START	65	I	SETUP	95	I	IC3
6	I	IB1	36	O	UPMOD	66	I	DCLIP	96	I	IC2
7	I	IB2	37	O	D0	67	I	ESR	97	I	IC1
8	I	IB3	38	O	D1	68	I	HUE	98	I	IC0
9	I	IB4	39	O	D2	69	I	YGAIN	99	I	PRT1
10	I	IB5	40	O	D3	70	I	CGAIN	100	I	CK27
11	—	GND	41	—	GND	71	—	GND	101	—	GND
12	I	IB6	42	O	D4	72	I	ADD	102	I	CF1
13	I	IB7	43	O	D5	73	I	DLMOD	103	I	VD1
14	I	IB8	44	O	D6	74	O	TOUT1	104	I	HD1
15	I	IB9	45	O	D7	75	O	TOUT2	105	I	IA11
16	—	V_{DD}	46	—	V_{DD}	76	—	V_{DD}	106	—	V_{DD}
17	I	HD2	47	O	D8	77	I	TS1	107	I	IA10
18	I	VD2	48	O	D9	78	I	TS2	108	I	IA9
19	I	CF2	49	O	D10	79	I	TS3	109	I	IA8
20	I	PRT2	50	O	D11	80	I	TS4	110	I	IA7
21	—	GND	51	—	GND	81	—	GND	111	—	GND
22	I	TLCH	52	O	HDOUT	82	O	EDGE1	112	I	IA6
23	I	ADR0	53	O	VDOUT	83	O	EDGE2	113	I	IA5
24	I	ADR1	54	O	CFO	84	I	PRT3	114	I	IA4
25	I	ADR2	55	O	PRTO	85	I	CF3	115	I	IA3
26	I	ADR3	56	I	OEN	86	I	VD3	116	I	IA2
27	O	INT0	57	I	YCS	87	I	HD3	117	I	IA1
28	O	VITC	58	I	SELECT	88	I	IC9	118	I	IA0
29	O	LTPLS	59	I	ROMTS	89	I	IC8	119	I	REFCF
30	O	PREND	60	—	V_{DD}	90	I	IC7	120	—	V_{DD}

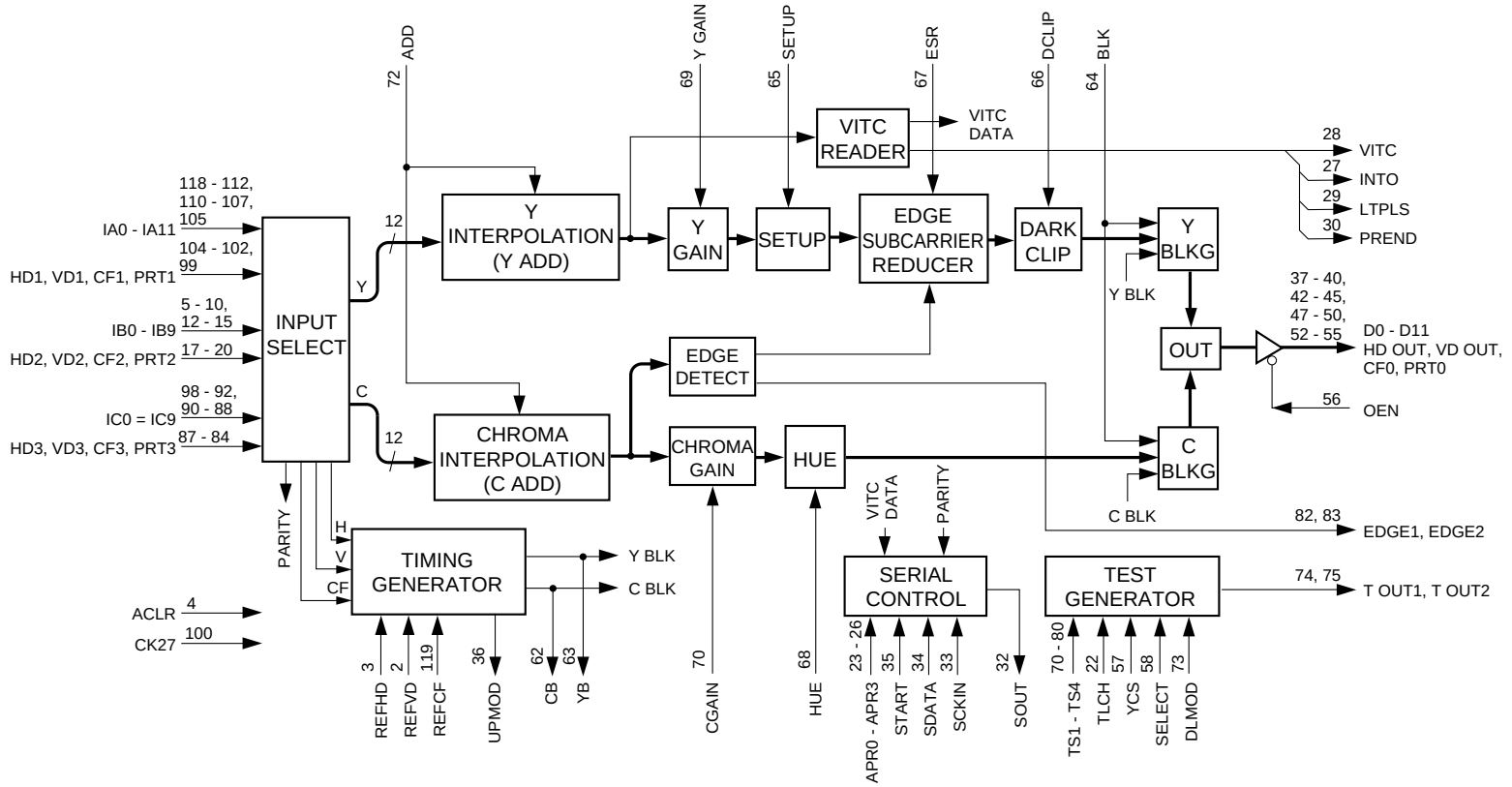


INPUT

ACLR ; RESET
ADD ; Y/C ADD ON
ADR0-ADR4
; IC ADDRESS
BLK ; BLKG ON
CF1-CF3 ; COLOR FRAMING FOR A, B, C INPUT
CGAIN ; C GAIN ON
CK27 ; 27 MHz CLOCK
DCCLIP ; DARK CLIP ON
DLMOD, ROMTS, SELECT, TLCH, TS1-TS4, YCS
; TEST TERMINAL
ESR ; EDGE SUBCARRIER REDUCER ON
HD1-HD3 ; HD FOR A, B, C INPUT
HUE ; HUE ON
IA0-IA11, IB0-IB9, IC0-IC9
; DATA A, B, C
OEN ; OUTPUT ENABLE
PRT1-PRT3
; PARITY FOR A, B, C INPUT
REFCF, REFHD, REFVD
; REFERENCE CF, HD, VD
SCKIN ; SERIAL COMMUNICATION CLOCK
SDATA ; SERIAL COMMUNICATION DATA
SETUP ; SETUP ON
START ; SERIAL COMMUNICATION START PULSE
VD1-VD3 ; VD FOR A, B, C INPUT
VGAIN ; Y GAIN ON

OUTPUT

CB ; C BLK PULSE TEST
CF0 ; COLOR FRAMING
D0-D11 ; DATA
EDGE1, EDGE2, LTPLS, PREND, TOUT1, TOUT2
; TEST TERMINAL
HDOUT ; HD
INTO ; INTERRUPT WHEN VITC READ
PRTO ; PARITY
SOUT ; SERIAL COMMUNICATION DATA
UPMOD ; MEMORY SHIFT MODE FOR Y-ADD
VDOUT ; VD
VITC ; VITC TEST
YB ; Y BLK PULSE TEST


ADD
72
Y GAIN
69
SETUP
65
ESR
67
DCLIP
66
BLK
64
VITC READER
VITC DATA
28
VITC
27
INTO
29
LTPLS
30
PREND
118 - 112, 110 - 107, 105
IA0 - IA11
104 - 102, 99
HD1, VD1, CF1, PRT1
5 - 10, 12 - 15
IB0 - IB9
17 - 20
HD2, VD2, CF2, PRT2
98 - 92, 90 - 88
IC0 = IC9
87 - 84
HD3, VD3, CF3, PRT3
INPUT SELECT
Y
C
12
12
Y INTERPOLATION (Y ADD)
Y GAIN
SETUP
EDGE SUBCARRIER REDUCER
DARK CLIP
Y BLKG
Y BLK
OUT
37 - 40, 42 - 45, 47 - 50, 52 - 55
D0 - D11
HD OUT, VD OUT, CF0, PRT0
56
OEN
EDGE DETECT
CHROMA INTERPOLATION (C ADD)
CHROMA GAIN
HUE
C BLKG
C BLK
82, 83
EDGE1, EDGE2
PARITY
H
V
CF
TIMING GENERATOR
Y BLK
C BLK
VITC DATA
PARITY
SERIAL CONTROL
TEST GENERATOR
74, 75
T OUT1, T OUT2
ACLR
4
CK27
100
3
REFHD
2
REFVD
119
REFCF
36
UPMOD
62
CB
63
YB
70
CGAIN
68
HUE
23 - 26
APR0 - APR3
35
START
34
SDATA
33
SCKIN
32
SOUT
70 - 80
TS1 - TS4
22
TLCH
57
YCS
58
SELECT
73
DLMOD