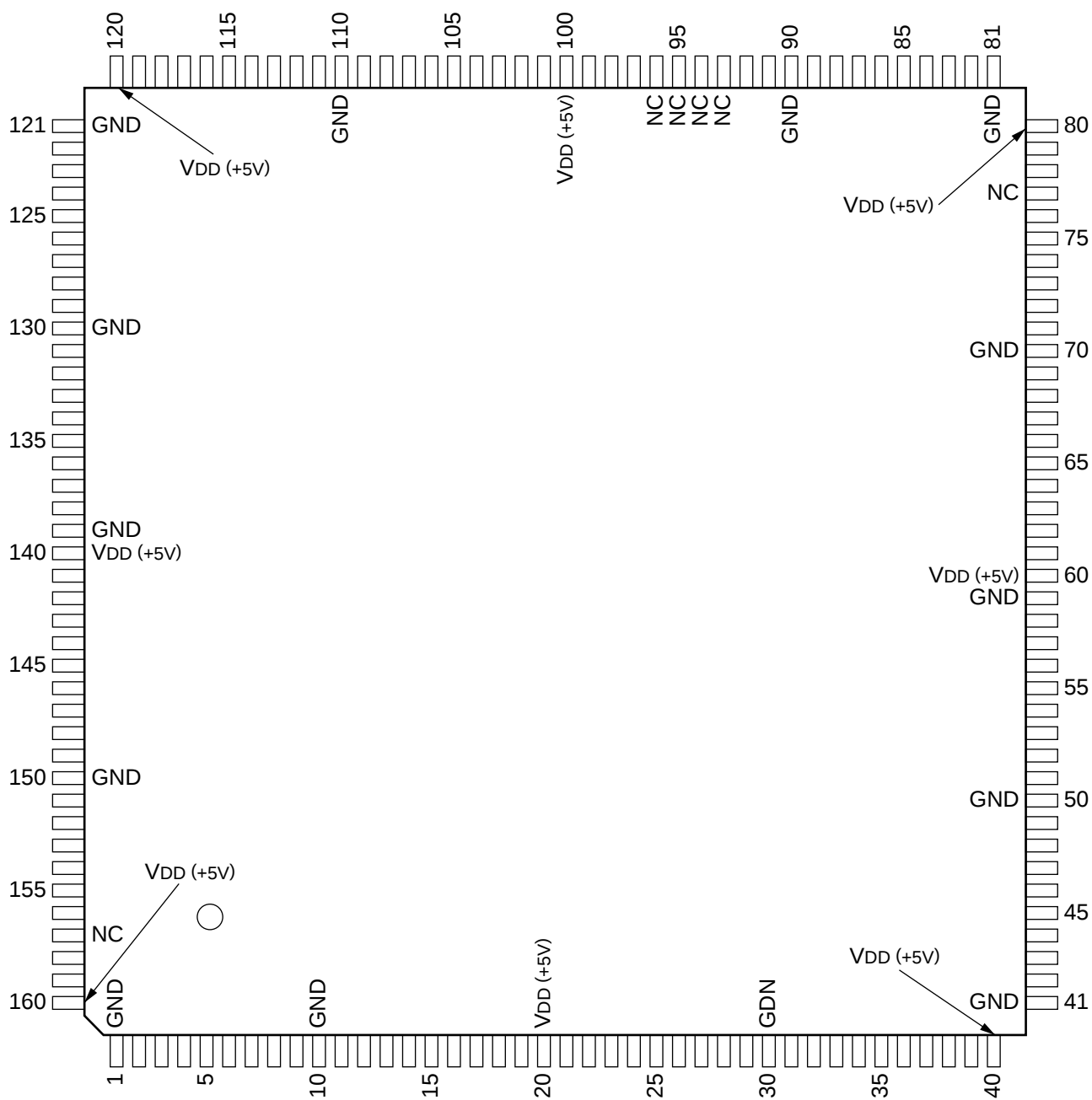

C-MOS POLAR COORDINATE CONVERTER

-TOP VIEW-



(VDD = +5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	33	I	D0	65	I	QRSL	97	I	AT0	129	O	Q13
2	O	P7	34	I	D1	66	I	RRND	98	I	AT1	130	—	GND
3	O	P8	35	I	D2	67	O	R2	99	I	AT2	131	O	Q14
4	O	P9	36	I	D3	68	O	R3	100	—	VDD	132	O	Q15
5	I	Y0	37	O	XSIGN	69	O	R4	101	I	AT3	133	O	QINT
6	I	Y1	38	O	YSIGN	70	—	GND	102	I	AT4	134	I	X2
7	I	Y2	39	O	XZERO	71	O	R5	103	I	AT5	135	I	X3
8	O	P10	40	—	VDD	72	O	R6	104	I	AT6	136	I	X4
9	O	P11	41	—	GND	73	I	CLR	105	I	AT7	137	I	X5
10	—	GND	42	O	YZERO	74	I	TIS0	106	I	AT8	138	I	CLK
11	O	P12	43	I	D4	75	I	TIS1	107	O	Q0	139	—	GND
12	O	P13	44	I	D5	76	I	TIS2	108	O	Q1	140	—	VDD
13	O	P14	45	I	D6	77	—	NC	109	O	Q2	141	I	X6
14	I	Y3	46	I	D7	78	O	R7	110	—	GND	142	I	X7
15	I	Y4	47	I	A0	79	O	R8	111	O	Q3	143	I	X8
16	I	Y5	48	I	A1	80	—	VDD	112	O	Q4	144	I	X9
17	I	Y6	49	I	WE0	81	—	GND	113	O	Q5	145	I	X10
18	I	Y7	50	—	GND	82	O	R9	114	I	AT9	146	I	X11
19	I	Y8	51	I	WE1	83	O	R10	115	I	AT10	147	O	P0
20	—	VDD	52	I	WE2	84	O	R11	116	I	AT11	148	O	P1
21	I	Y9	53	I	WE3	85	I	TOS0	117	I	AT12	149	O	P2
22	I	Y10	54	I	FNC0	86	I	TOS1	118	O	Q6	150	—	GND
23	I	Y11	55	I	FNC1	87	I	TOS2	119	O	Q7	151	O	P3
24	I	Y12	56	I	PCMP	88	O	R12	120	—	VDD	152	O	P4
25	I	Y13	57	I	PMOD	89	O	R13	121	—	GND	153	I	X12
26	I	Y14	58	I	PRND	90	—	GND	122	O	Q8	154	I	X13
27	I	Y15	59	—	GND	91	O	R14	123	O	Q9	155	I	X14
28	O	P15	60	—	VDD	92	O	R15	124	O	Q10	156	I	X15
29	O	EQ	61	O	R0	93	—	NC	125	I	X0	157	—	NC
30	—	GND	62	O	R1	94	—	NC	126	I	X1	158	O	P5
31	O	YBIG	63	I	PTHR	95	—	NC	127	O	Q11	159	O	P6
32	O	SIGN	64	I	QRND	96	—	NC	128	O	Q12	160	—	VDD

[illegible]

INPUT

A0, A1 ; CPU ADDRESS
 AT0 - AT12 ; NEGATIVE/POSITIVE CONNECTION EXTERNAL ROM DATA
 CLK ; CLOCK
 CLR ; 0 = XC, YC, PROT, PCNT REGISTER CLEAR
 D0 - D7 ; CPU DATA
 FNC0, FNC1 ; FUNCTION SELECT
 PCMP ; 1 = AT REGISTER USE
 PMOD ; 0 = ROM 8/1 = ROM 13
 PRND ; 1 = P ROUND UP NUMBERS OF FIVE AND ABOVE AND ANYTHING UNDER FIVE
 PTHR ; 1 = ROM NON-COMPENSATION
 QRND ; 1 = Q ROUND UP NUMBERS OF FIVE AND ABOVE AND ANYTHING UNDER FIVE
 QRSL ; 0 = Q BIT-0 ROUND UP NUMBERS OF FIVE AND ABOVE AND ANYTHING UNDER FIVE
 1 = Q BIT-2 ROUND UP NUMBERS OF FIVE AND ABOVE AND ANYTHING UNDER FIVE
 RRND ; 1 = R ROUND UP NUMBERS OF FIVE AND ABOVE AND ANYTHING UNDER FIVE
 TIS0 - TIS2 ; TEST INPUT SELECT
 TOS0 - TOS2 ; TEST OUTPUT SELECT
 WE0 - WE3 ; CPU DATA WRITE ENABLE
 X0 - X15 ; CROSS COORDINATES X SIGNED/UNSIGNED FIXED-POINT WITH 4 BIT FRACTION
 Y0 - Y15 ; CROSS COORDINATES Y SIGNED/UNSIGNED FIXED-POINT WITH 4 BIT FRACTION

OUTPUT

EQ ; XD = YD : 1
 P0 - P15 ; POLAR COORDINATES θ ANGLE
 Q0 - Q15 ; FRACTIONAL PART OF QUOTIENT EXTERNAL ROM ADDRESS
 Q INT ; INTEGRAL PART OF QUOTIENT
 R0 - R15 ; POLAR COORDINATES γ RADIUS
 SIGN ; XD, YD = MINUS : 1
 XSIGN ; XD = MINUS : 1
 XZERO ; XD = ZERO : 1
 YBIG ; XD, YD COMPARE (XD < YD = 1)
 YSIGN ; YD = MINUS : 1
 YZERO ; YD = ZERO : 1
 0 ; LOW LEVEL
 1 ; HIGH LEVEL

