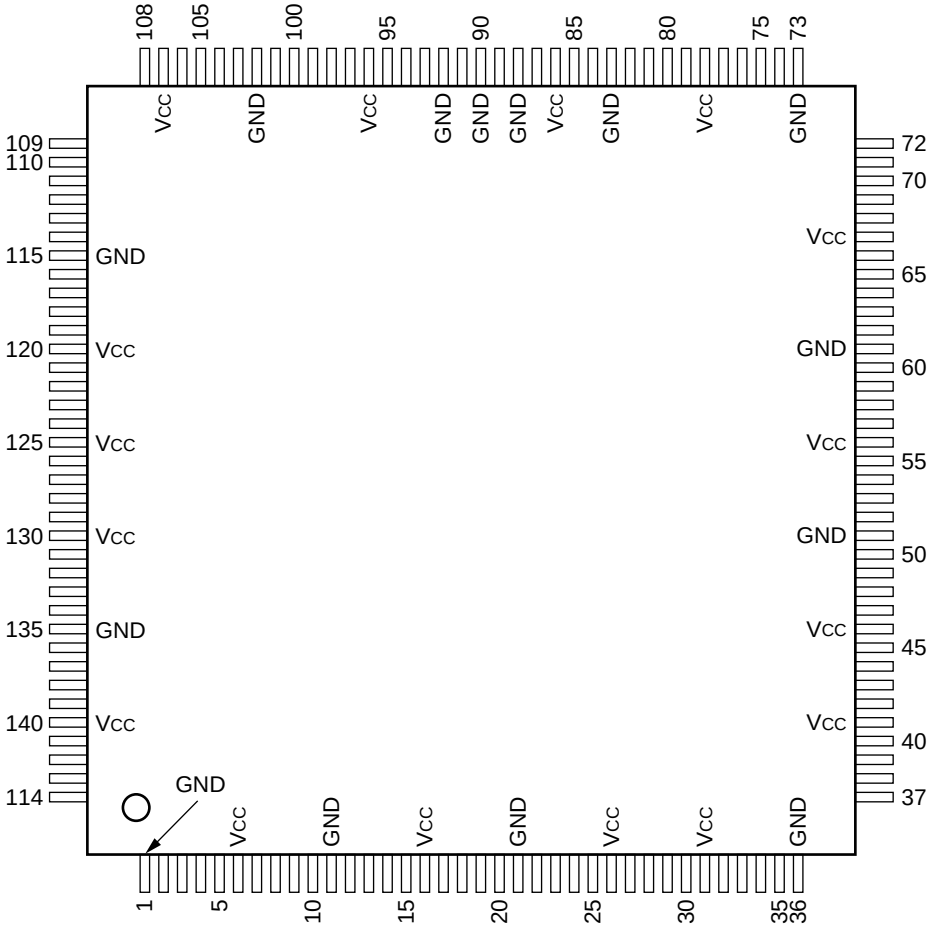
CAMLINK

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	37	O	FMSWCK	73	—	GND	109	O	MCCLK
2	I	DSPYIN0	38	O	FMRSTW	74	I/O	PHD7	110	I	MCB8B16
3	I	DSPYIN1	39	O	FMWEEV	75	I/O	PHD6	111	I/O	MCDATA0
4	I	DSPYIN2	40	O	FMWEOD	76	I/O	PHD5	112	I/O	MCDATA1
5	I	DSPYIN3	41	—	Vcc	77	I/O	PHD4	113	I/O	MCDATA2
6	—	Vcc	42	I	FMQEV0	78	—	Vcc	114	I/O	MCDATA3
7	I	DSPYIN4	43	I	FMQEV1	79	I/O	PHD3	115	—	GND
8	I	DSPYIN5	44	I	FMQEV2	80	I/O	PHD2	116	I/O	MCDATA4
9	I	DSPYIN6	45	I	FMQEV3	81	I/O	PHD1	117	I/O	MCDATA5
10	I	DSPYIN7	46	—	Vcc	82	I/O	PHD0	118	I/O	MCDATA6
11	—	GND	47	I	FMQEV4	83	—	GND	119	I/O	MCDATA7
12	I	DSPCIN0	48	I	FMQEV5	84	I/O	PHCTL1	120	—	Vcc
13	I	DSPCIN1	49	I	FMQEV6	85	I/O	PHCTL0	121	I/O	MCDATA8
14	I	DSPCIN2	50	I	FMQEV7	86	—	Vcc	122	I/O	MCDATA9
15	I	DSPCIN3	51	—	GND	87	I	PHSCLK	123	I/O	MCDATA10
16	—	Vcc	52	I	FMQOD0	88	—	GND	124	I/O	MCDATA11
17	I	DSPCIN4	53	I	FMQOD1	89	O	PHLREQ	125	—	Vcc
18	I	DSPCIN5	54	I	FMQOD2	90	—	GND	126	I/O	MCDATA12
19	I	DSPCIN6	55	I	FMQOD3	91	I	CKTESTEN	127	I/O	MCDATA13
20	I	DSPCIN7	56	—	Vcc	92	—	GND	128	I/O	MCDATA14
21	—	GND	57	I	FMQOD4	93	I	MSNTBIHIZ	129	I/O	MCDATA15
22	I	/DSPHD	58	I	FMQOD5	94	O	MSNTOUT	130	—	Vcc
23	I	/DSPVD	59	I	FMQOD6	95	I	MSNTCLK	131	I	/MCCS
24	I	DSPFLD	60	I	FMQOD7	96	—	Vcc	132	O	/MCCA
25	I	DSPCK	61	—	GND	97	O	CYST	133	I	/MCWR
26	—	Vcc	62	O	FMSRCK	98	I	MCADD0	134	O	/MCINT
27	O	FMD0	63	O	FMRSTR	99	I	MCADD1	135	—	GND
28	O	FMD1	64	O	FMREEV	100	I	MCADD2	136	O	MCARXD
29	O	FMD2	65	O	MSRSV	101	I	MCADD3	137	O	MCPREARXD
30	O	FMD3	66	O	FMREOD	102	—	GND	138	I	MCBUSY
31	—	Vcc	67	—	Vcc	103	I	MCADD4	139	I	MCDMAEN
32	O	FMD4	68	O	GRFEMP	104	I	MCADD5	140	—	Vcc
33	O	FMD5	69	O	POWERON	105	I	MCADD6	141	O	MCISOACT
34	O	FMD6	70	O	MSCYLOUT	106	I	MCADD7	142	O	CYDNE
35	O	FMD7	71	I	MSCYLIN	107	—	Vcc	143	I	/MSDMARST
36	—	GND	72	I	MSRAMEZ	108	I	MCBCLK	144	I	/RESET

INPUT

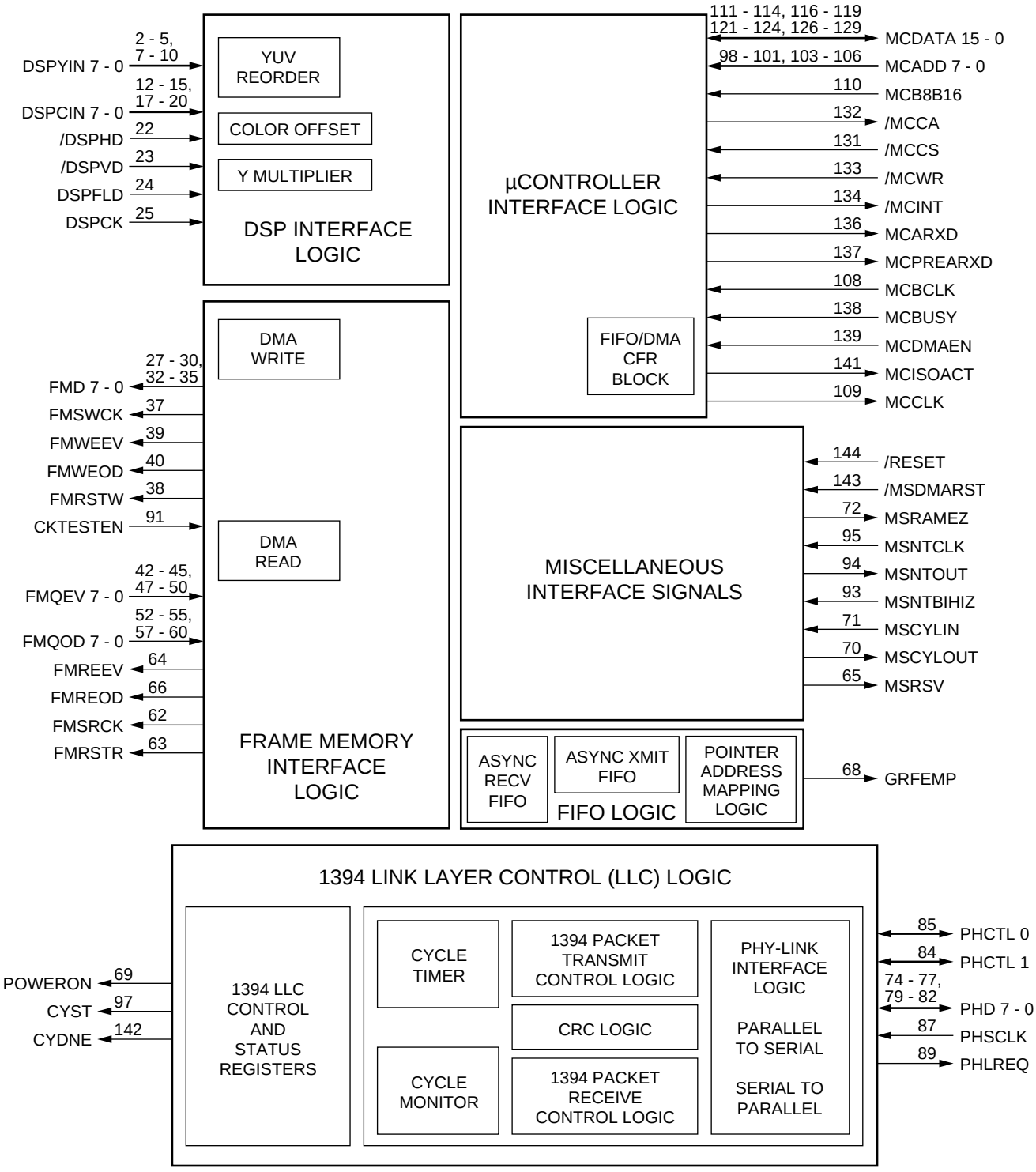
/DSPHD	:	HORIZONTAL SYNCHRONIZATION SIGNAL
/DSPVD	:	VERTICAL SYNCHRONIZATION SIGNAL
/MCCS	:	CYCLE START TO LINK
/MCWR	:	WRITE/READ INDICATOR TO LINK
/MSDMARST	:	RESET (ACTIVE LOW)
/RESET	:	RESET (ACTIVE LOW)
CKTESTEN	:	WDMA TEST CLOCK ENABLE
DSPCIN 7 - 0	:	VIDEO DATA
DSPCK	:	DSP OUTPUT SYNCHRONIZATION CLOCK
DSPFLD	:	ODD/EVEN FIELD INDICATOR
DSPYIN 7 - 0	:	VIDEO DATA
FMQEV 7 - 0	:	EVEN FIELD MEMORY FIFO DATA ON FMSRCK WHEN FMRE
FMQOD 7 - 0	:	ODD FIELD MEMORY FIFO DATA ON FMSRCK WHEN FMRE
MCADD 7 - 0	:	ADDRESS BUS, MCADD 0 IS MS BIT
MCB8B16	:	DATA BUS WIDTH SELECTOR
MCBCLK	:	HOST BUS CLOCK SUPPLIED TO LINK
MCBUSY	:	MICROCONTROLLER BUSY INDICATOR
MCDMAEN	:	ISO DMA ENABLE USED WITH ISOSTEN IN CFR 0×54 BIT 6
MSCYLIN	:	CYCLE INPUT
MSNTBIHIZ	:	NAND TREE BIDIRECTIONAL 3-STATE OUTPUT
MSNTCLK	:	NAND CLOCK
MSRAMEZ	:	RAM 3-STATE ENABLE
PHSCLK	:	SYSTEM CLOCK

OUTPUT

/MCCA	:	CYCLE ACKNOWLEDGE FROM LINK
/MCINT	:	INTERRUPT TO MICROCONTROLLER
CYDNE	:	ISO CYCLE DONE INDICATOR
CYST	:	ISO CYCLE START INDICATOR
FMD 7 - 0	:	DATA PRESENTED TO FIELD MEMORY FIFO FOR STORAGE
FMREEV	:	INCREMENTS FIELD MEMORY READ ADDRESS POINTER FOR EVEN FIELD
FMREOD	:	INCREMENTS FIELD MEMORY READ ADDRESS POINTER FOR ODD FIELD
FMRSTR	:	RESET FIELD MEMORY READ ADDRESS POINTER TO ZERO
FMRSTW	:	RESET FIELD MEMORY WRITE ADDRESS POINTER TO ZERO
FMSRCK	:	MEMORY READ CLOCK 1/2 READ CLOCK (25.000 MHz)
FMSWCK	:	MEM 1/2 WRITE CLOCK (17.025 MHz/12.285 MHz)
FMWEEV	:	ENABLE WRITE EVEN FIELD FIFO AND INCREMENT ADDRESS POINTER ON FMSWCK
FMWEOD	:	ENABLE WRITE ODD FIELD FIFO AND INCREMENT ADDRESS POINTER ON FMSWCK
GRFEMP	:	GRF EMPTY INDICATOR
MCARXD	:	ASYNC PACKET RECEIVED INDICATOR FROM INTERNAL CONFIGURATION REGISTER (CFR)
MCCLK	:	MICROCONTROLLER CLOCK IS SYSCLK/4
MCISOACT	:	DMA STATUS
MCPREARXD	:	PRE ASYNC PACKET RECEIVED INDICATOR FROM CONFIGURATION REGISTER (CFR)
MSCYLOUT	:	CYCLE OUTPUT
MSNTOUT	:	NAND TREE OUTPUT
MSRSV	:	RESERVED
PHLREQ	:	LINK REQUEST
POWERON	:	LINK POWER ON INDICATOR

INPUT/OUTPUT

MCDATA 15 - 8	:	LS BYTE OF DATA BUS, MCDATA 8 IS MS BIT
MCDATA 7 - 0	:	MS BYTE OF DATA BUS, MCDATA 0 IS MS BIT
PHCTL 1, 0	:	CONTROL 1 AND 0 OF THE PHY-LINK CONTROL BUS
PHD 7 - 0	:	DATA 7 TO 0 OF THE PHY-LINK DATA BUS


DSPYIN 7 - 0
2 - 5, 7 - 10
DSPCIN 7 - 0
12 - 15, 17 - 20
/DSPHD
22
/DSPVD
23
DSPFLD
24
DSPCK
25
YUV REORDER
COLOR OFFSET
Y MULTIPLIER
DSP INTERFACE LOGIC
µCONTROLLER INTERFACE LOGIC
FIFO/DMA CFR BLOCK
111 - 114, 116 - 119
121 - 124, 126 - 129
MCDATA 15 - 0
98 - 101, 103 - 106
MCADD 7 - 0
110
MCB8B16
132
/MCCA
131
/MCCS
133
/MCWR
134
/MCINT
136
MCARXD
137
MCPREARXD
108
MCBCLK
138
MCBUSY
139
MCDMAEN
141
MCISOACT
109
MCCLK
DMA WRITE
DMA READ
FMD 7 - 0
27 - 30, 32 - 35
FMSWCK
37
FMWEEV
39
FMWEOD
40
FMRSTW
38
CKTESTEN
91
FMQEV 7 - 0
42 - 45, 47 - 50
FMQOD 7 - 0
52 - 55, 57 - 60
FMREEV
64
FMREOD
66
FMSRCK
62
FMRSTR
63
FRAME MEMORY INTERFACE LOGIC
MISCELLANEOUS INTERFACE SIGNALS
144
/RESET
143
/MSDMARST
72
MSRAMEZ
95
MSNTCLK
94
MSNTOUT
93
MSNTBIHIZ
71
MSCYLIN
70
MSCYLOUT
65
MSRSV
ASYNC RECV FIFO
ASYNC XMIT FIFO
POINTER ADDRESS MAPPING LOGIC
FIFO LOGIC
68
GRFEMP
1394 LINK LAYER CONTROL (LLC) LOGIC
1394 LLC CONTROL AND STATUS REGISTERS
CYCLE TIMER
CYCLE MONITOR
1394 PACKET TRANSMIT CONTROL LOGIC
CRC LOGIC
1394 PACKET RECEIVE CONTROL LOGIC
PHY-LINK INTERFACE LOGIC
PARALLEL TO SERIAL
SERIAL TO PARALLEL
POWERON
69
CYST
97
CYDNE
142
85
PHCTL 0
84
PHCTL 1
74 - 77, 79 - 82
PHD 7 - 0
87
PHSCLK
89
PHLREQ