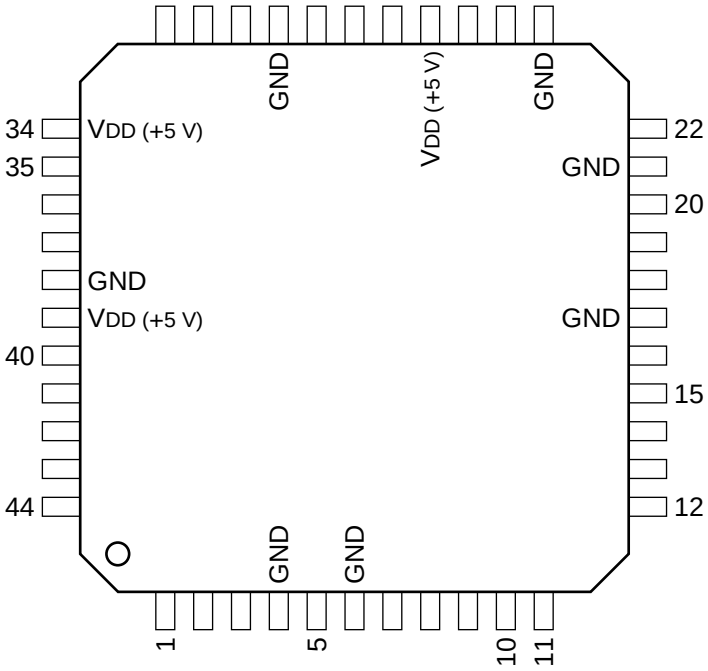
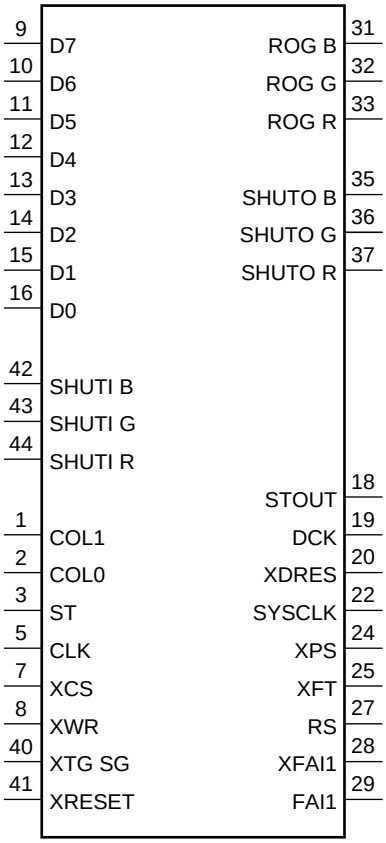
C-MOS GATE ARRAY

—TOP VIEW—





(VDD = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	COL1	12	I	D4	23	—	GND	34	—	VDD
2	I	COL0	13	I	D3	24	O	XPS	35	O	SHUTO B
3	I	ST	14	I	D2	25	O	XFT	36	O	SHUTO G
4	—	GND	15	I	D1	26	—	VDD	37	O	SHUTO R
5	I	CLK	16	I	D0	27	O	RS	38	—	GND
6	—	GND	17	—	GND	28	O	XFAI1	39	—	VDD
7	I	XCS	18	O	STOUT	29	O	FAI1	40	I	XTG SG
8	I	XWR	19	O	DCK	30	—	GND	41	I	XRESET
9	I	D7	20	O	XDRES	31	O	ROG B	42	I	SHUTI B
10	I	D6	21	—	GND	32	O	ROG G	43	I	SHUTI G
11	I	D5	22	O	SYSCLK	33	O	ROG R	44	I	SHUTI R